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Application Research of FPGA-DSP Architecture in Ship Radar Signal Processing

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Abstract. In view of the continuous improvement of maritime safety requirements, the demand for maritime radar signal processing system is increasing day by day. A ship radar Signal processing system based on Field-Programmable Gate Array (FPGA) and Digital Signal Processor (DSP) is designed in this paper. The system design covers the construction of hardware architecture and the realization of signal processing algorithm. Through the advantages of FPGA in parallel processing and logic realization, and the powerful ability of DSP in high-speed mathematical operation and signal processing algorithm, the high-speed data interaction of ship and ship system is realized. The stability of the system is verified by simulation and measured data. The results show that the system can effectively process the radar echo signal, realize the rapid and accurate detection of Marine targets, and perform well in clutter suppression. The design of this paper not only meets the needs of modern ship radar signal processing, but also provides a new idea and technical reference for the research of related fields.

Keywords. Radar signal processing; FPGA+DSP; Parallel processing; Clutter suppression; Marine target detection

1. Introduction

With the rapid development of China's Marine economy and industry, as well as the promotion of national strategies such as "One Belt, One Road" and "Marine Power Strategy", the application of ship radar signal processing technology in maritime transportation, ports and ships has become increasingly important[1]. There is a growing need for autonomous and controllable technology, especially in the critical area of ship-to-ship radar signal processing, which is critical to national security. Under the current research background, this paper focuses on the application of ship radar signal processing system in improving the accuracy and real-time detection of targets. Through in-depth analysis and optimization of existing algorithms, it aims to provide efficient and reliable technical support for Marine detection[2].

Digital signal processing plays a core role in radar system, and FPGA and DSP are the key hardware to realize digital signal processing[3]. Zuo Lin uses TMS320 C6678

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DSP to implement a multi-beam radar signal processing architecture, which utilizes multi-core consistency, EDMA3 transmission and message queuing technology to achieve efficient multi-core synchronization. This design reduces the storage resource consumption of DSP and simplifies the design of subsequent filters[4]. Despite these advances, monolithic processing units still have room for improvement in processing speed. Zhang designed a radar signal detection system for "low, slow and small" targets. Using heterogeneous architecture of FPGA and DSP, XC7K410T chip and TMS320C6678 chip are specifically adopted to design advanced algorithms for radar echo signals, and ping-pong transmission is adopted to read and write echo data, ensuring real-time data flow and high efficiency of processing[5]. However, faced with the increasingly complex electromagnetic environment, there is still room for further optimization of clutter suppression algorithms.

Drawing from these research findings, this paper introduces a shipborne radar signal processing system that utilizes a combination of FPGA and DSP technology. The high-performance chips of Fudan Micro JFM7K325T and Feiten FT-M6678 are selected. The architecture design of the system is discussed in detail from three aspects: system function division, hardware design implementation and signal processing flow. The feasibility of the system is verified by combining the simulation experiment with the measured data. Finally, this paper summarizes the research results.

2. System scheme design

As the core part of the radar system, the radar signal processing system is responsible for converting the original signal received by the radar antenna into useful information that can be used for target detection, tracking and recognition. The signal processing architecture mainly consists of modules such as signal acquisition, pre-processing, signal processing and display control platform[6]. The signal processing architecture is shown in Figure 1.

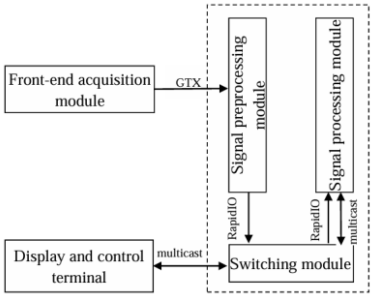

Figure 1. Signal processing architecture

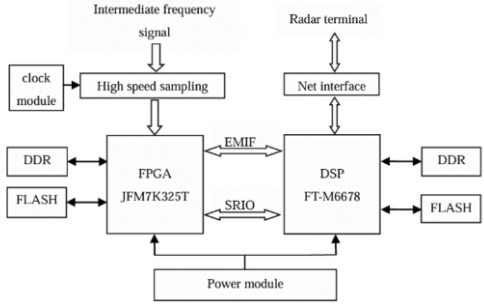

Figure 2. Radar hardware composition

The hardware framework of the signal processing system is shown in Figure 2. The front-end A/D sampling module integrates an AD9467 chip, which provides excellent linearity without an external voltage reference source or driver.

The signal preprocessing module uses Fudan Micro FPGA chip to process the sampled data of A/D module, and performs pulse compression, DBF and down-conversion processes. The processed signal is transmitted through the RapidIO protocol to the DSP module, which is responsible for clutter suppression, target detection, parameter calculation and feature extraction to improve signal quality and information extraction. The processing results are sent to the display control terminal through

Ethernet, and the terminal also sends control instructions to the DSP through Ethernet, including adjusting radar parameters, optimizing signal processing algorithms, etc., to adapt to tasks and environmental changes. The specific flow of signal processing is shown in Figure 3.

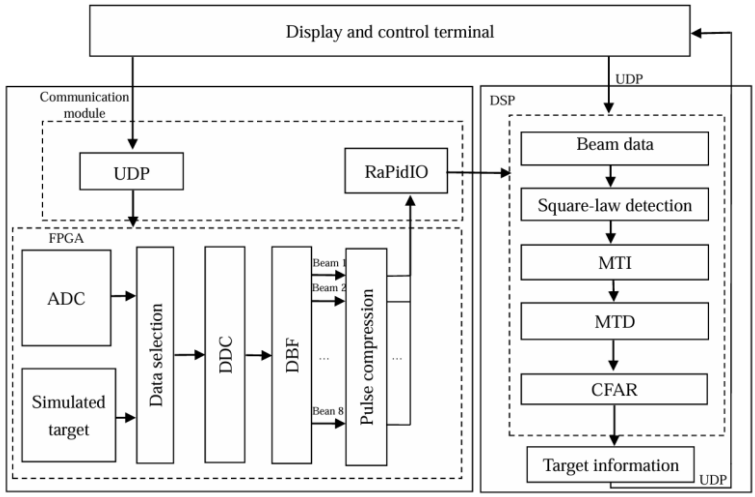

FIG 3. Algorithm flow of signal processing system

3. System implementation

3.1. Hardware design

1) SRIO design

The FT-M6678 chip has a pair of independent serial Fast Output (SRIO) interfaces. In differential signal transmission, impedance matching can be achieved by connecting suitable inductors in series in the line, thus effectively transmitting the differential signal while suppressing high-frequency noise and signal reflection. Figure 4 shows the interconnection between the FT-M6678 SRIO and the FPGA.

The chip needs to convert high-speed serial signals into 100MHz level digital signals, is responsible for handling data transmission inside and outside the chip, and supports 8-core shared use. The system adopts GTX interface 4x1 serial mode with a rate of 3.125Gbps, uses four sets of differential pairs to connect two high-speed interfaces, and connects the transceiver line accordingly [7]. Table 1 shows the configuration of the SRIO transmission rate.

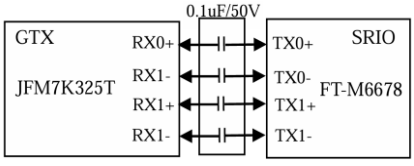

Figure 4. SRIO circuit connection

Table 1. Description of the SRIO transmission rate

Configuration mode	value
1.25Gbps	3'h0
2.5Gbps	3'h1
3.125Gbps	3'h2
Retain (default)	3'h3

2) EMIF design

An External Memory Interface (EMIF) is an interface between external memory and other on-chip units.

The EMIF main frequency is CPU/10 frequency, 1GHz device, main frequency is 100mhz. The wiring diagram of the system EMIF and 32-bit SRAM/NOR flash memory chip is shown in Figure 5. EMIFD has multiple data pins to support bidirectional parallel data transfer. EMIFA is an external address output that specifies the memory address to be accessed by the DSP to facilitate data read and write operations. EMIFCE provides signals for chip storage space, while at high power levels, external storage is disabled[8].

The EMIF is internally entered in bytes, and the address unit of the port EMIFA output is consistent with the ASIZE setting of the CE space configuration register.

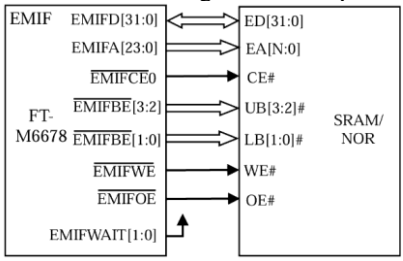

Figure 5. EMIF connection diagram

3.2. Signal processing flow

1) Digital orthogonal down conversion

To prevent spectrum aliasing, the sample rate of the LFM pulse signal should be at least twice its maximum frequency, although this guarantees the signal quality, but increases the hardware cost and data processing burden. With digital down-conversion (DDC) technology, we can convert the IF signal to the baseband signal and reduce the sampling rate. The key steps of DDC include orthogonal transformation, filtering, and extraction, which converts the real signal into a complex signal for easy subsequent processing[9]. In the digital mixing orthogonal transformation, the input signal is transformed into discrete signal by analog-to-digital converter, and then multiplied with two orthogonal local oscillator signals, filter out the high frequency, get the digital baseband signal, and finally get the orthogonal signal by extraction. The system block diagram of the above process is shown in Figure 6.

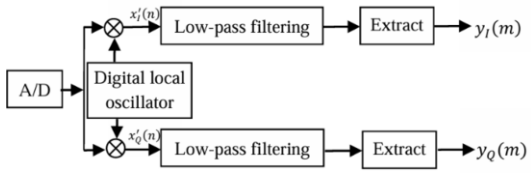

Figure 6. DDC structure diagram

The input IF analog signal can be expressed as:

$$x_s(t) = a(t)\cos\left(2\pi f_0 t + \theta(t)\right) \tag{1}$$

$a(t)$is the analog signal amplitude, and $\theta(t)$ is the analog signal phase.

After the input IF signal is quantized by A/D, it can be expressed as:

$$x(n) = a(n)\cos\left(2\pi \frac{f_0}{f_s} n + \theta(n)\right) \tag{2}$$

Multiply with the digital orthogonal local oscillator $\omega_0 = 2\pi \frac{f_0}{f_s}$ respectively to obtain the I/Q channel mixing signal:

$$x_I'(n) = a(n)\cos(2\omega_0 n + \theta(n)) + a(n)\cos(\theta(n)) = x_{IH}(n) + x_I(n) \quad (3)$$

$$x_Q'(n) = -a(n)\sin(2\omega_0 n + \theta(n)) + a(n)\sin(\theta(n)) = x_{QH}(n) + x_Q(n) \quad (4)$$

Therefore, by filtering out the high-frequency components $X_{IH}(n)$、$X_{QH}(n)$, the in-phase and orthogonal components $x_I(n)$、$x_Q(n)$ of zero IF signal can be obtained, which not only significantly reduces the amount of data in signal processing.

4. Test results and verification

The pcb of the system in this paper is shown in Figure 7. It is necessary to carry out various performance tests of the system, including system simulation test and field experiment.

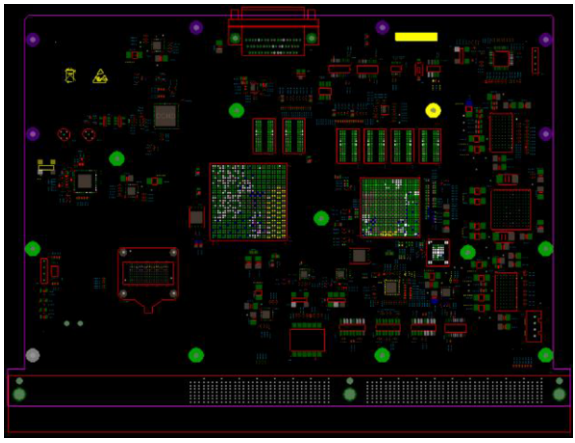

FIG 7. System PCB Layout Diagram

4.1. Object detection function verification

In MATLAB environment, the radar echo signal is simulated according to the actual sys tem parameters, and it is imported into FT-M6678 DSP for signal processing to verify it s target detection capability.

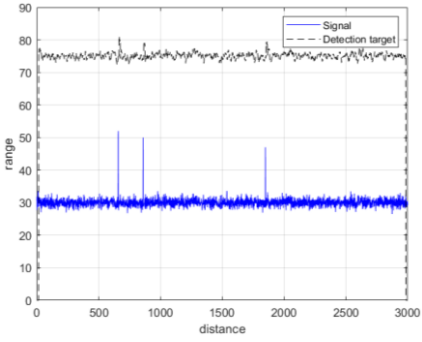

FIG 8. MATLAB pulse pressure data

Table 2. MATLAB simulation pulse Doppler echo signal parameters

Work parameter	Numerical	unit
Working frequency	9.5	GHz
Signal bandwidth	15	MHz
Pulse width	4	μs
Maximum speed	10	m/s
Distance element	5	m
Velocity resolution	1	m/s

In order to simulate the combination of long and short pulses in the actual system, the pulse width of the transmitted waveform is set to 4μs, which corresponds to the distance blind area of 600 meters. After the analog echo signal is generated by MATLAB, the pulse compression is carried out to obtain the data shown in Figure 8. The numerical table of simulation parameters is shown in Table 2. The echo signal contains three targets, the distance of each target relative to the radar is 660m, 860m and 1850m, and the radial velocity is -5m/s, 4m/s and 8m/s, respectively.
Simulation data, real distance test results and errors are shown in Table 3.

Table 3. Comparison of test results

No.	True Value	Test Value	Error	True Value	Test Value	Error
		Distance (m)			Speed (m/s)	
1	660	654	0.91%	-5	-4.89	2.2%
2	860	873	1.51%	4	4.06	1.5%
3	1850	1868	0.97%	8	8.17	2.13%

After the simulated pulse compression data is processed by DSP program, the parameters of the three detected targets are basically consistent with those of the simulated targets, and the distance error is up to 1.51% and 2.2% respectively. For this system, the error is acceptable. The above verifies the correctness of the signal processing program in DSP.

4.2. Field test results

During the test, the antenna is initially aimed at the sea surface, and the transmitter sends radar pulses that bounce back as echo signals when it encounters an object. The system then processes these echoes, applying techniques such as coherence integration to improve the signal-to-noise ratio, and using a constant false alarm rate (CFAR) algorithm to minimize false detections. Finally, the test results are recorded in a data file. The radar scanning diagram during terminal operation is shown in Figure 9.

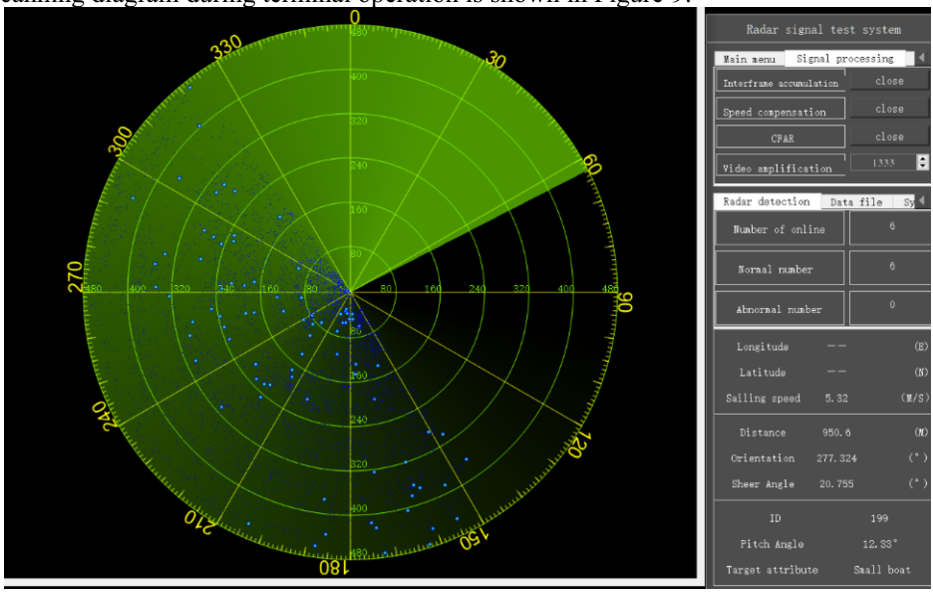

FIG 9. Radar scan of field test

The test results show that through signal processing technology, the radar system can accurately detect the distance, direction and speed of the target ship, and can effectively and stably track small ships, and the generated track is very close to the actual sailing track of the ship, indicating that the radar performance meets the expected requirements and can accurately monitor and track the maritime target.

5. Conclusion

According to the detection principle of ship radar, a set of ship radar signal processing system based on FPGA+DSP is designed to realize the acquisition of echo signal, digital down conversion and constant false alarm algorithm processing, which effectively reduces the burden of data transmission and improves the range resolution and detection accuracy of radar. MATLAB is used to verify the correctness of the signal processing program. The distance error is less than 1.51%, and the speed error is less than 2.2%. In addition, the reliability of the signal processing system is proved by field test. The test results show that this system can accurately locate the measured target, and the designed system has strong stability, good real-time performance and superior detection performance, which has important engineering application value.

Acknowledgment

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