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A Low Power Test Data Compression Scheme for Scan Test

Bo YE[1]
Shanghai Educational Technology Centre, Shanghai, China

Abstract. In this paper, an uncertain state filling method is proposed, which can not only effectively reduce the scan shifting power consumption, but also reduce the test time simultaneously for scan test. This method is based on the threshold algorithm of uncertain state filling, which can both reduce weighted transitions metric (WTM) and improve compression efficiency for test vectors. Experiments with ISCAS'89 benchmark circuits show that the proposed algorithm can make a good tradeoff between power consumption and compression efficiency.

Keywords. Low power, test data compression, scan test

1. Introduction

As integrated circuit design enters the nano stage, the scale is getting larger and larger, and the power consumption of design and test will bring serious problems [1]. Usually, the problem of test power consumption mainly includes excessive peak power consumption and average power consumption [2]. It is reported that the power consumption of the chip during the scan test is much higher than the normal working mode, which will damage the chip during the scan test, resulting in a reduction in yield [3]. Therefore, more attention should be paid to the power consumption during scan test, so that the test power consumption cannot exceed the threshold. With the increase of SoC's integration and complexity, the test time and cost will also increase significantly [4]. The amount of test data and test time are two other serious problems in SoC testing.

At present, there have been many researches on controlling the amount of test data, test time and power consumption. Test power consumption can be reduced by utilizing low-transition test pattern generators [1] [5-7], test vector reconstruction [8], modification of scan chains [9-10], and build-in-self test (BIST) [11-13]. The low-transition scheme reduces power consumption by assigning a fixed value to the uncertain position in the test channel, or mapping the don't cares to '0' or '1' according to special rules, thus reducing the number of transitions. Test vector reordering technology rearranges the scan latch and test vector, which can improve the power consumption. Scan chain modification technology reduces scan power by modifying structure of scan chains, thus it brings more extra hardware overhead. BIST structures are more suitable for IP core testing, with high fault coverage and low test cost [14].

[1] Corresponding Author, Ye Bo, Shanghai Educational Technology Centre, 1541, Da Lian Rd., Shanghai, China; E-mail: yebo925@126.com.

However, BIST takes a long test time, and it is mainly used for memory testing and is not suitable for general chips.

Test compact [15-16] and test compression techniques [17-20] can be used to reduce the amount of test data and test time. Test compaction technology can reduce the number of test vectors without reducing the fault coverage. But the compacted test sets may cause some physical defects to be undetectable [21]. Test compression technology can reduce the amount of test data and test time, but most of them can't reduce test power simultaneously.

With test data grows fast in large SoCs, the rapid growth of test data increases the test time and power consumption, which leads to the increase of chip test cost, and the increase of power consumption will damage the chip in the test process and bring reliability problems. However, rare methods can significantly improve compression efficiency and reduce power consumption at the same time.

This paper proposes an uncertain state filling algorithm, which can improve the compression efficiency and reduce the power consumption simultaneously. The algorithm can efficiently map the uncertain state to the appropriate determined state 0 or 1, and greatly reduce the test vector's switch activities. It provides a solution that can reduce the test volumes, test time and test power consumption.

2. Uncertain State Filling Algorithm

2.1. Switching Activity in EDT Environment

Scan test power consumption includes shift power consumption and response capture power consumption. Fig.1 shows the embedded deterministic test (EDT) structure.

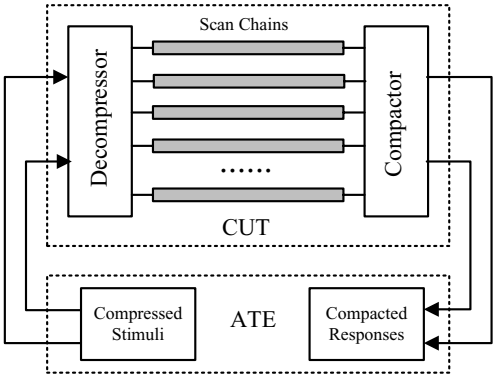

Figure 1. EDT structure.

As shown in Figure 1, the automatic test equipment (ATE) stores compressed test patterns and expected test responses. The compressed test vectors are transmitted to the de-compressor in a continuous manner through external channels during test. The circuit under test (CUT) compacts the test responses and then delivers them to ATE. The scan shifting power is directly dependent on the number of transitions that occur in the scan chains.

2.2. Power Dissipation Model

For CMOS circuits, most of the circuit power consumption is consumed in the conversion process of circuit components from logic 0 to 1 or from logic 1 to 0. During chip testing, the state change of circuit components is closely related to the change of test vectors. When the original inputs or scan flip-flops change the value, these components will switch [22]. Therefore, the scan test power consumption is closely related to the number of transitions of the test vector. Those with more transition times consume more power.

A model for estimating the power consumption of scan test is proposed in 16]. The scan power consumption is related not only to the number of transitions of the test vector, but also to the positions of 0 and 1 in the test vector. For example, for the test vector *v1v2v3v4* = 0100, where *v1* is the first vector, and the transition from 0 to 1 in this vector brings more switching behavior than the transition from 1 to 0. The shift power consumption during test can be estimated in the same way. More studies show that transition power consumption plays a major role in test power consumption.

For a scan test sequence $t_j = t_{j,1}, t_{j,2}, \ldots, t_{j,l}$, where l is the length of the scan chain and $t_{j,1}$ is the first scan vector. The weighted transitions metric (WTM) [23] for t_j is given by

$$\mathrm{WTM}_j = \sum_{i=1}^{l-1} (l-i)(t_{j,i} \oplus t_{j,i+1}) \tag{1}$$

For a given test set, the peak and average power consumption can be estimated by the following formulas:

$$P_{avg} = \frac{\sum_{j=1}^{n} \sum_{i=1}^{l-1} (l-i)(t_{j,i} \oplus t_{j,i+1})}{n} \tag{2}$$

$$P_{peak} = \max_{j \in \{1,2,\ldots n)} \left\{ \sum_{i=1}^{l-1} (l-i)(t_{j,i} \oplus t_{j,i+1}) \right\} \tag{3}$$

From equations (2), (3), it is obviously that the key to reducing power consumption is to reduce the number of transitions of the test vectors and the weight l - i.

2.3. Lower Power Uncertain State Filling Algorithm

For the alternate variable run-length coding [4], to lower the power dissipation and achieve high test compression efficiency, the mapping of don't cares need to consider the value of WTM, the longest length of runs of 1's and 0's, and the least number of consecutive 1's and 0's. The solution is like an N-P complete problem.

To solve the above problem, we introduce the concepts of run factor α and alternate factor β, and we will quickly get the better leverage of power dissipation and compression efficiency. The α is the ratio of real run-length and longest expected run-length. The $\alpha \in [0,1]$, and α indicates that the 1's or 0's can get its longest run-length when it equals to value '1'. i.e., for test vectors "00XXX11XX10", run length of 0's is

mapped in expected manner, and the prime test sequence is then mapped to "000001,11110". It is easy to get the longest run of 0's is 5. But if the prime vector is mapped to "001,11111110", then we get the longest run of 1's and its value is 8. So if the prime test sequence is mapped to "00001,111110" during the algorithm executing process, then the run factor for 0's is α_0=4/5=0.8, and the run factor for 1's is α_1=6/8=0.75.

Alternate factor β indicates the alternating status of 0 and 1 in test sequence. If all 1 and 0 appear alternately, that is there are no consecutive 0's or 1's, then β=1, and no separator is needed. If the longest 0's or 1's after mapping is S, then β=1/S, and there are no consecutive 0's or 1's when S=1. The smaller the β, the higher efficiency the test data compression will be.

The don't care mapping models can be shown as following:

$$C_{avg} = \frac{\beta P_{avg}}{\alpha_0 \alpha_1} = \frac{\beta \sum_{j=1}^{n} \sum_{i=1}^{l-1} (l-i)(t_{j,i} \oplus t_{j,i+1})}{n \alpha_0 \alpha_1} \tag{4}$$

$$C_{peak} = \frac{\beta P_{peak}}{\alpha_0 \alpha_1} = \frac{\beta \max\limits_{j \in \{1,2 \ldots n\}} \left\{ \sum_{i=1}^{l-1} (l-i)(t_{j,i} \oplus t_{j,i+1}) \right\}}{\alpha_0 \alpha_1} \tag{5}$$

In (4), (5), C_{avg} is the evaluate parameter of average power and compression efficiency. C_{peak} is the evaluate parameter of peak power and compression efficiency. α_0 and α_1 are run factor for 0's and 1's respectively, and β is the alternating factor.

3. Experimental Results

ISCAS'89 full scan circuit is used to verify and compare the compression effect, test time and test power consumption. For the convenience of comparison, every circuit is designed by a single scan chain. Table 1 shows the comparison results for the ISCAS'89 benchmarks for test sets obtained from the Mintest ATPG program between the uncertain state filling technology, the FDR code [24] and the AVR algorithm [5] where T_D is the original test set.

Table 2 shows the comparison between the experimental results of test power consumption using the algorithm in this paper and TRP technology [25], including test peak power consumption and average power consumption. P_{peak} and P_{avg} are the peak and average power dissipation obtained with compacted test sets from the Mintest program. Compared with TRP [25] algorithm, the average reduction of peak power consumption of this algorithm is 38.49%, and the average reduction of average power consumption is 42.37%. It is obvious from Table 2 that this algorithm can not only significantly improve the compression effect, but also significantly reduce the test power consumption.

Table 1. Comparison of compression obtained using T_D

Circuit	Size of T_D (bits)	FDR code (bits) [24]	AVR Code (bits) [5]	This work	
				bits	Percentage Compression
S5378	23754	12346	9233	8856	62.72
S9234	39273	22152	16129	14476	63.14
S13207	165200	30880	23896	19080	88.45
S15850	76986	26000	19388	17761	76.93
S38417	164736	93466	51679	42074	74.46
S38584	199104	77812	57142	48621	75.58

Table 2. Comparison of scan-in power consumption

Circuit	TRP [25]		This work			
	P_{peak}	P_{avg}	P_{peak}	P_{peak} Reduction (%)	P_{avg}	P_{avg} Reduction (%)
S5378	9531	2435	5651	40.71	1459	40.08
S9234	12060	3466	6158	48.94	1673	51.73
S13207	97606	7703	58765	39.79	4576	40.59
S15850	63478	13381	38973	38.60	8055	39.80
S38417	404617	112198	230046	43.14	61013	45.62
S38584	479530	88298	384691	19.78	56184	36.37
Average	-	-	-	38.49	-	42.37

4. Conclusion

We have presented an efficient don't care bit mapping algorithm which can effectively reduce SoC test power dissipation, test volume and test time simultaneously. By introducing the concepts of run factor α and alternate factor β to get the better leverage of the power dissipation and compression efficiency, the corresponding estimation models of power dissipation are also proposed. Experimental results indicate that the uncertain state filling technique is not only effective for the scan shifting power reduction, but also has better test data compression ratio.

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