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Study of Work-Function Variation on Performance of Dual-Metal Gate Fin Field-Effect Transistor

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Abstract. The impact of work-function variation (WFV) on performance of an inversion-mode (IM) dual-metal gate (DMG) fin field-effect transistor (FinFET) was investigated for the first time. The statistical fluctuations induced by WFV on the threshold-voltage (V_{TH}), transconductance (g_m), and subthreshold slope (SS) were demonstrated and estimated utilizing a 3D technology computer-aided design (TCAD) simulator. We found that the performance variations of the DMG FinFET were affected by two different metals near the drain and near the source, respectively. Additionally, this effect of the two metals on the channel was not monotonic with the length of the channel of their own control. Our work fills a gap in the study of WFV for a DMG IM FinFET and provides a reference for optimizing the distribution of the two metals.

Keywords. Work-function variation; fin field-effect transistor; dual-metal gate; process variation

1. Introduction

With the continuous scaling of a semiconductor device size, the short channel effects (SCEs) and gate transport inefficiency become more and more serious; this means that the gate-to-channel control becomes worse and worse [1–3]. To counter these undesired barriers, high-k materials (such as HfO_2) replaced the traditional SiO_2 as the oxide layer material at sub-45 nm technology node to avoid the occurrence of gate leakage current being larger than the subthreshold leakage [1]. In addition, a metal gate has substituted for polysilicon because of the incompatibility between polysilicon and high-k materials. However, the use of metal gate inevitably introduces work-function variation (WFV). This is because the work-function (WF) of each metal grain depends on its own crystalline orientations and is difficult to control during metal gate deposition [4–7].

Meanwhile, a FinFET with silicon fin as one of the most promising candidates has attracted much attention in recent years; this is because the fin-based devices have high carrier mobility and a great control over the carriers in the channel, and are excellent in suppressing SCEs [8–10]. To further improve the FinFET's performance, the structure of the dual-metal gate (DMG) has been proposed for advanced devices [11-12]. Instead of the single-metal gate (SMG), dual-metal gates (DMG; i.e., Metal gate 1 'M1', near

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the source, and Metal gate 2 'M2', near the drain) with different WFs are used on the gate stack. According to related studies, DMG can not only suppress SCEs and simultaneous transconductance (g_m) improvement, but can also improve current drive capability compared with the SMG structure due to different WFs in the metal gate [3, 10–16]. Meanwhile, different manufacturing methods for DMG structure have also been studied, and the new DMG structure requires only additional processing steps to laterally form two well-controlled contacting metal materials [12, 17].

In nanoscale integrated devices, WFV as one of major random variation sources has been of enormous interest for high-K/metal gate technology [18–21]. The effect of WFV on the SMG has already been well reported. However, knowledge of its influence on the DMG is still missing. Therefore, we investigate, for the first time, the impact of WFV on the performance of DMG FinFET. The different ratios of the length of the M1, also named as control gate to that of the total gate on device performance fluctuation caused by WFV are also explored. Therefore, we study to provide a reference for optimizing the distribution of the two metals in the design of FinFETs.

2. Device Structure and Simulations

Fig. 1 shows a bird's eye view of a DMG IM FinFET, which is used in the present study. The detailed structural information for the DMG FinFET is as follows: a fin height of 16 nm, a channel length of 20 nm, a fin width of 5 nm, and a gate oxide thickness of 2 nm. In addition, a uniform donor doping concentration of 1×10^{19} cm^{-3} in the drain and source regions is used, and 1×10^{16} cm^{-3} acceptor particles are doped in the channel. TiN and TaN are chosen as the metals of M1 and M2, respectively. According to requirements of DMG, the WF of M1 is bigger than that of M2. As shown in Fig. 1, it illustrates three different WFs of TaN (4.0 eV, 4.15 eV, and 4.8 eV) depending on three possible grain orientations (<100>, <200>, and <220>) with different probabilities of occurrences (50%, 30%, and 20%) and two possible WFs of TiN (4.6 eV and 4.4 eV), owing to two different grain orientations (<100> and <111>) with two probabilities of occurrences (60% and 40%) [1]. It is noted that TiN is a well-known gate metal used in an SMG n-channel device, and TaN is not suitable as a metal gate for the SMG n-channel device. The length of the channel under control gate M1 is $L1$; while the length of the channel under screen gate M2 is $L2$; and the total gate length is L = 20 nm. Fig. 2 gives a cross section along the channel of the studied IM DMG FinFET.

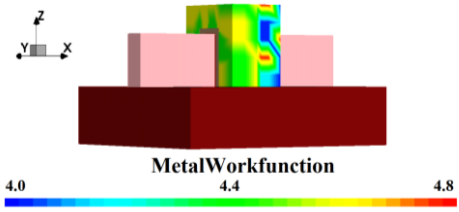


Fig. 1 Schematic diagram of the simulation of WFV of DMG FinFET.

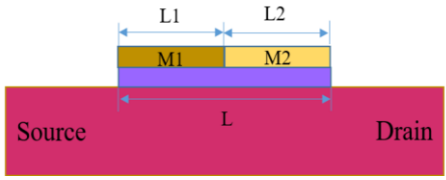
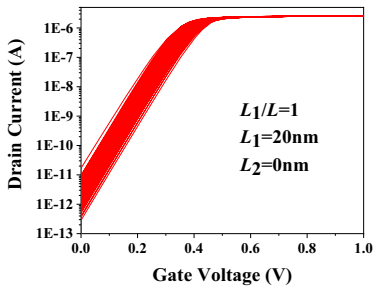


Fig. 2 Cross section along the y-axis at y = 0. The gate near the source is also named as the "control gate", and the gate near the drain is also named as the "screen gate."

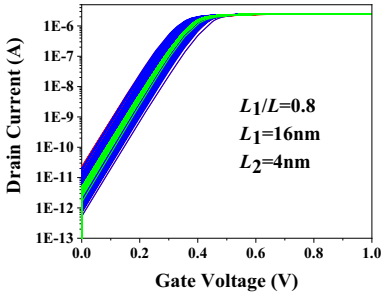
To accurately investigate the impact of the ratio of the length of different control gates on the performance fluctuation caused by WFV in the IM DMG FinFET, we carefully let L_1/L be 0, 0.2, 0.4, 0.6, 0.8 and 1. It is worth mentioning that the device can be considered to be an SMG with TaN and TiN only as gate stack at L_1/L = 0 and 1, respectively.

3. Results and Discussions

The impact of WFV on the electrostatic integrity of the DMG IM FinFET is shown by the dispersion of the transfer curve in Figs. 3 (a)–(f). The figures give input characteristic curves of drain current against gate voltage (V_{GS}) at drain voltage (V_{DS}) = 50 mV for each case. In these figures, the red curves represent the WFV-induced variation of performance in the case of S1; the green ones represent the case of S2; and the blue ones represent the S3 situation. As shown by the area occupied by the discrete curves that is getting larger and larger, WFV-induced electrostatic integrity fluctuations in the IM DMG FinFET becomes more serious, which is at L_1/L from 0.8 to 0.2. This means that the value of L_1/L has a bad effect on the WFV-induced variability in the DMG IM FinFET. More especially, when L_1/L is from 1 to 0.2 in steps of -0.2, the green and red curves occupy an increasing area significantly; this means that drain current's dispersion is getting worse. Furthermore, the standard deviation of V_{TH}, the subthreshold slope (SS), the saturation current (I_{sat}), and g_m were calculated for each case. To better analyze the experimental results, the relative standard deviations of the relevant parameters of the DMG IM FinFET were also calculated.



(a)



(b)

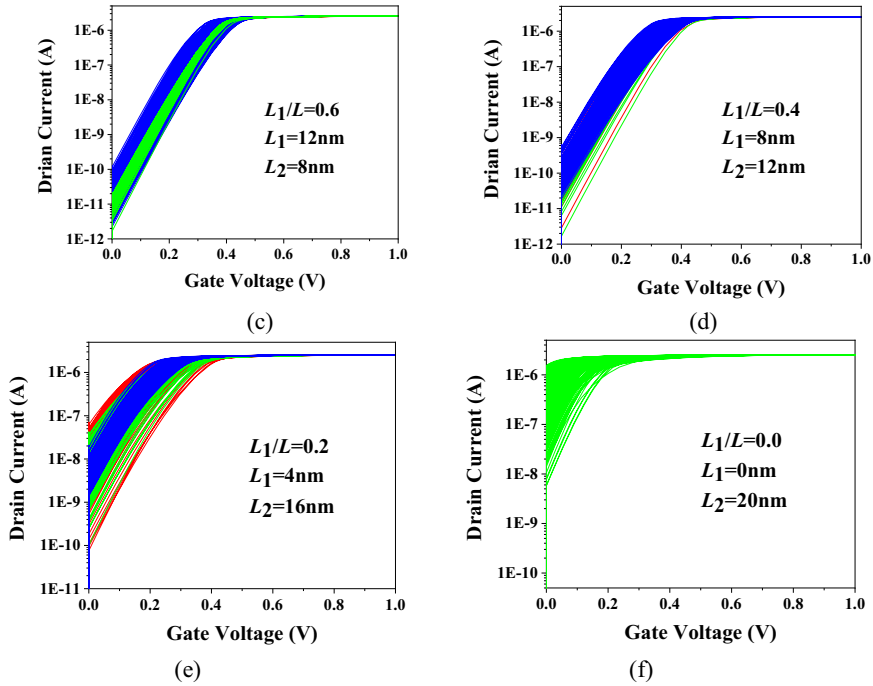
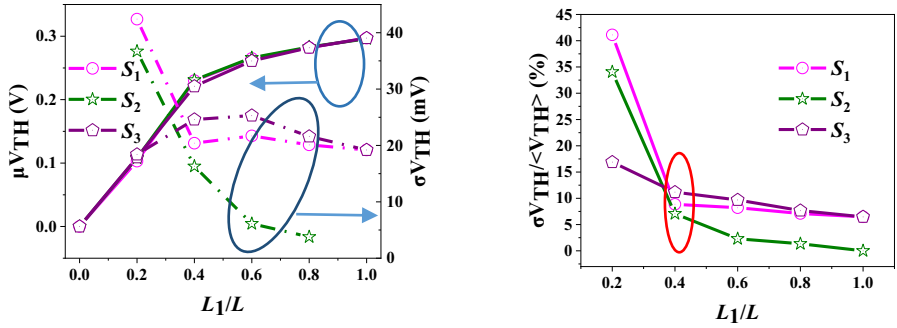


Fig. 3 WFV-induced variations of drain current versus V_{GS} for an IM DMG FinFET.

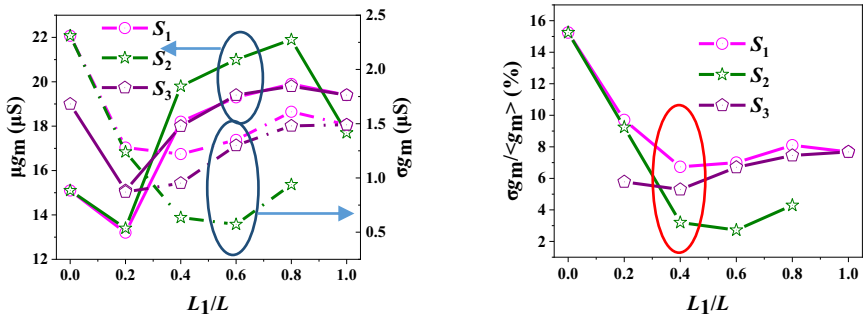
The V_{TH} has been extracted by the constant-current method at a fixed current of 0.1 μA/μm. These values are shown in Figs. 4, 5, and 6. In these figures, it should be noted that off-state current is greater than 0.1 μA/μm at L_1=0[22]. Therefore, V_{TH} is defined as 0 V, and the missing value of SS. Therefore, our study verifies that TaN cannot be used alone as the metal gate for an n-channel FinFET. In the Fig. 4 (a), as the value of L_1/L keeps getting smaller, the WFV-induced variability becomes worse as the average value of V_{TH} becomes smaller. In cases S1, S2 and S3, when L_1/L is from 0 to 1, the average values of V_{TH} are almost equal (see the solid line in Fig. 4 (a)). At the same time, when L_1/L is from 1 to 0.4, in the case of S1, the V_{TH} fluctuation caused by WFV is similar to that in case S3, but the V_{TH} fluctuation caused by case S1 is similar to that by case S2 (see the red circle in Fig. 4 (b)) when L_1/L is less than 0.4. At the same time, it is interesting that when L_1/L is between 0.4 and 1, the effect of WFV on the V_{TH} in case S1 is smaller than that in case S3. This indicates that the WFVs of M1 and M2 are not independent of each other; on the contrary, for the same L_1/L, the WFV of M2 has a certain inhibitory effect on the WFV of M1.



(a) (b)

Fig. 4 The average and standard deviation of V_{TH} variations caused by WFV at different values of L_1/L.

The characteristics of g_m in Figs. 5 (a) and (b) for DMF FinFET with different L_1/L values are shown. Similar to the case of V_{TH}, when L_1/L is from 1 to 0.4 in steps of -0.2, the g_m fluctuation caused by WFV in the case of S1 is similar to that in the case of S3, but when L_1/L is less than 0.4, the g_m fluctuation caused by case S1 is similar to that by case S2 (see the red circle in Fig. 5 (b)). Moreover, the g_m characteristic of the device no longer simply increased or decreased as L_1/L decreases; when L_1/L is larger than 0.4, the g_m value of DMG is generally greater than the g_m value of SMG with TiN as the MG, which means that the ability of g_m for DMG IM FinFET is improved at this time, and g_m reaches the maximum at L_1/L = 0.8. Moreover, when L_1/L is greater than 0.4, the fluctuation of g_m decreases slightly as L_1/L decreases.

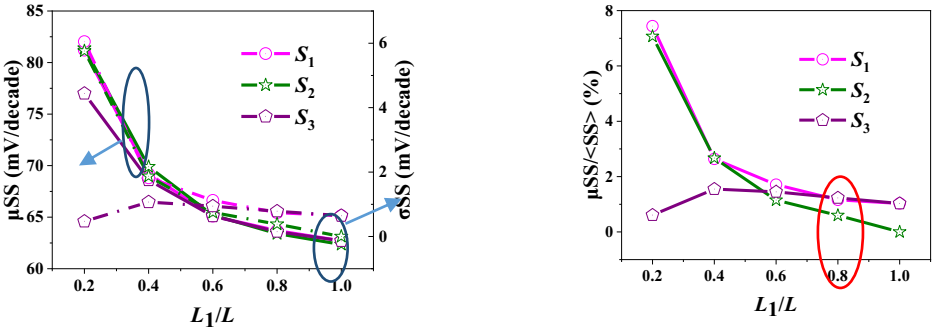


(a) (b)

Fig. 5 Average and standard deviation of g_m variations caused by WFV at different values of L_1/L.

The SS characteristics in Figs. 6 (a) and (b) of the DMG FinFET are shown in steps of 0.2 at L_1/L from 0 to 1. It is observed that the DMG FinFET has a bigger SS compared to a corresponding SMG FinFET with TiN. It can be attributed to the SS for a transistor is inversely proportional to its effective length [23], and the effective length of the DMG device is only slightly bigger than that of L_1 in the subthreshold region. By contrast, the effective length of the SMG device is slightly bigger than the total channel length [3]. Inevitably, since we set L_1/L from 0 to 1 in the present study, L_1 is less than or equal to L. The effective length decreases with a decrease in L_1/L or L_1. Therefore, the SS of the DMG FinFET device increases gradually (see the solid line in Fig. 5 (a)).

When L_1/L is from 1 to 0.6 in steps -0.2, in case S1, the WFV-induced SS fluctuation is similar to that in case S3, but when L_1/L is smaller than 0.6, the SS variability caused by the case S1 is similar to that of case S2 (see the red circle in Fig. 6 (b)). When L_1/L is from 0.4 to 1, the rise and SS variability is not large, but when L_1/L is less than 0.4, the value and fluctuation of SS increase sharply.



(a) (b)

Fig. 6 The average and standard deviation of SS variations caused by WFV at different values of L_1/L.

Generally, although the WFV of M1 has a strong impact on the performance fluctuation for the DMG FinFET, this effect is weakened as L_1 decreases. Meanwhile, the effect of M2, which is relatively weak in causing device parameter variations for the DMG FinFET, gradually becomes stronger when the length L_2 increases. Even when L_1/L is less than 0.4, the WFV-induced device performance fluctuations by MG of M2 gradually dominate the device performance fluctuation caused by the entire MG WFV. Additionally, when L_1/L is less than 0.4, the influence of TaN's WFV on the device begins to dominate. Therefore, for the DMG FinFET, it is necessary to ensure that L_1/L is greater than a certain amount. Furthermore, at this time, because the metal work function of M1 is dominant, the channel region under M2 has greater optimization freedom. For example, the substrate doping can be reduced in this region, thereby increasing the benefit that source and drain capacitance can be reduced, while potentially increasing the speed of the device [12]. In addition, some studies have considered $L_1/L = 0.5$ to be a suitable amount when they do not take the effect of WFV into account. However, our observations indicate that due to the WFV, the amount of L_1/L should be slightly bigger than 0.5 when WFV is considered. Also, it can reduce the performance variation caused by misalignment of the two gates.

4. Conclusion

For the first time, the impact of WFV-induced performance variability in DMG device has been explored in this study. It can be observed that the WFV from the M1 metal gate near the source is the main factor causing the device performance fluctuation.. Moreover, simulation results show that the fluctuation caused by WFV gradually becomes serious after a smaller WF metal gate is introduced near the drain. In addition, the performance fluctuations of the DMG FinFET caused by WFV are not monotonic by the change of L_1/L. Rather, as L_1/L decreases, the fluctuation of device performance

rises dramatically. From the perspective of the WFV, the introduction of a second metal in the gate has an obvious impact on the device performance of the DMG FinFET as L_1/L is smaller than 0.5. Therefore, increasing the value of L_1/L appropriately is reasonable.

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