Applied Mathematics, Modeling and Computer Simulation
C.-H. Chen et al. (Eds.)

doi:10.3233/ATDE240833

Low-Power VLSI Adiabatic Circuits for Bio-Medical Application

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Abstract. The paper reviews the application of VLSI in Bio-Medical electronics. It highlights the development of VLSI in micro-electronics such as pacemakers. The concept of VLSI is combined with the advantages of Adiabatic Circuits to develop a power-efficient method for Pacemakers. Basic measurements such as Power consumption, Drive Current and Area of the circuit are tracked. A schematic for reducing the power required to drive the circuit to the stability of a system using Adiabatic Logic is proposed. For this purpose, a simulation is performed highlighting the efficiency of the circuit. Further efficiency improvements for future models and schematics are outlined

Keywords. VLSI; adiabatic circuits; pacemaker, area; power efficiency; simulation

1. Introduction

Cardiac Pacemakers are implantable devices used to generate a rhythm for slow-beating hearts. Cardiac Pacemakers are being developed at a rapid rate and the need of power efficient is increasing. The application of pacemakers requires the device to be miniaturised which needs a small battery as the power source in the implementation side. This issue causes a need for frequent replacement in an unfavourable environment. A typical pacemaker circuit has an analog component that consists of a Low Noise Amplifier which needs to amplify the extremely low voltages produced by the heart also known as the QRS complex. The digital components include a Programmable Logic Control to monitor the rate at which the pacemaker operates, A timing clock circuit that is set to the heart rhythm and algorithms that decide the optimal heart rate. The pacemaker circuits are implemented using VLSI by creating CMOS amplifiers, clock circuits and PLCs. The devices are put under a low power condition making the logic of adiabatic circuits practical. Adiabatic circuits utilize an approach of reversible computing where the energy spent is reused rather than dispersed. The Adiabatic model introduces a high amount of power saving which is crucial in the application of pacemakers. This paper proposes an adiabatic implementation of an OP-AMP amplifier that plays a critical role in the functioning of a pacemaker

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2. Problem statement

Pacemakers are an essential part of cardiac healthcare providing a vital role in the sustainability of patients suffering from weak heart muscles. A research paper which surveyed patients in the Czech Republic [1,2] highlights the impact of COVID-19 on heart-related problems and the eventual utilization of pacemakers. Gender differences and age proved to be major factors in the need for the implantation of a pacemaker. The paper also discusses the limitation of care taken to these pacemakers. The need for a long-lasting pacemaker is evident from the data provided through the survey.

Data collected from a study in the United States [3] gives us an insight into the condition of implanted pacemakers in the United States. A survey of 450,000 people showed that about 0.26% or about 3 people in 1000 utilize pacemakers of any sort, which significantly rises over the ages of 70 and above. About 20% of these pacemakers have been replaced twice. This effect can be caused due to the low battery life of the pacemaker.

3. Literature review

Many authors have contributed in the domain of Adiabatic circuits, with each paper providing a different execution of the logic. Multiple papers were also published on the various implementations of CMOS pacemakers, A few of these papers are discussed below. Samik Samanta., et al. (2020) [4] proposed a second-order adiabatic logic model for a full adder. The 2PADCL provided a greater efficiency of power saving but consumed more area. Deepti Singhal et al. (2017) [5] provided power clocks for adiabatic circuits highlighting the various techniques that can be utilized to regenerate power. However, the various clocking techniques were not implemented in any use cases. Ishita Khindri et al. (2022) [6] utilized the adiabatic circuit methodology to implement a low-power ALU using wave-shaping diodes. The paper discusses various adiabatic methods and implements them in a digital circuit. The application of these logics in analog circuits is absent. Minakshi Sanadhya et al (2022) [7] proposed an adiabatic logic shift register for the use case of low-power IoT devices the paper goes through the various types of registers present and the implementation of each one in VLSI. This paper also does not discuss the implementation of this logic in analog circuits.

Long Yang et al (2014) [8] proposed a 680nm leadless pacemaker design implementing the design using an ECG acquisition IC. The publication highlights the various amplifiers and digital circuits necessary for a pacemaker and provides insights on the design. M Daliri et al (2008) [9] proposed a CMOS VLSI implementation of a Switched OP-AMP, Switched Capacitor Pacemaker. Various components were detailed and tested.

4. Methodology of adiabatic circuits

Adiabatic circuits work on the principle of charging and discharging based on the clock cycle of the input voltage. The circuit charges power when the clock moves from low

to high this phase is the Evaluate phase and discharges when the clock moves from high to low or the Recovery phase. The logic can be implemented through capacitors or can be enhanced by the addition of CMOS inverters to the existing logic. There are many existing advanced adiabatic concepts such as Positive Feedback Adiabatic Logic (PFAL) and Efficient Charge Recovery Logic (ECRL), but the basic working methodology remains the same throughout the various concepts. The clock cycle and its phases are described in Figure.1.

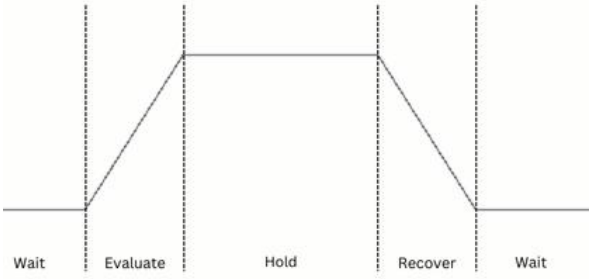

Figure 1. Operation of an adiabatic system

In non-adiabatic CMOS systems, a majority of the power dissipation is caused by the dynamic power dissipation through capacitances. In general, this dissipation can be mitigated significantly through adiabatic logic [10,11]. Assuming the power supplied is VDD and the capacitance of the system is C. We know that,

$$P = \frac{1}{2} C V_{DD}^2 \tag{1}$$

In an adiabatic system since the voltage supplied is varying there is a time constant the power also depends on the charging time of the capacitor.

$$P = \frac{1}{2T} C V_{DD}^2 \tag{2}$$

Where T is the charging time of the capacitor, by making sure the charge time is significant (greater than 2RC) we can provide an energy dissipation lesser that conventional CMOS. This is the fundamental principle for adiabatic charging. The general adiabatic logic circuit is represented in Figure 2. We can observe that the capacitor undergoes charging and discharging cycles based on the dynamic source voltage

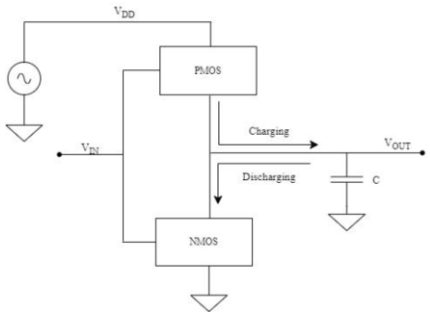

Figure 2. Circuit diagram of a general adiabatic model

5. Design of circuit

The Switched OP-Amp circuit is designed using a switched CMOS design[12]. The transistors are 45nm in size making them consume less area. A clock runs through the CMOS to avoid unnecessary turning off of the NMOS as shown in Figure 3. that are grounded. The non-grounded NMOS act as diodes, aiding the consistency of the Common Mode Voltage through the amplifier. The connected NMOS in the circuit help increase the gain of the amplifier. The PMOS stage is present in the input side to reduce noise and is switched on and off periodically through the provided clock [9,13].

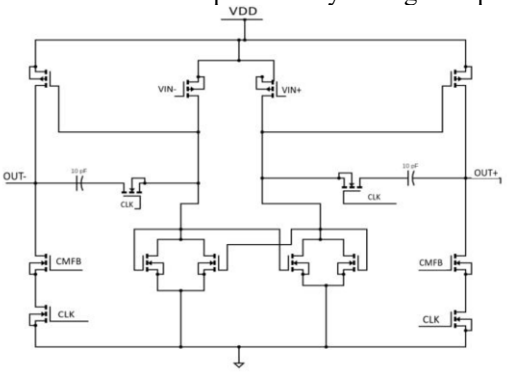

Figure 3. OP-Amp circuit

The adiabatic logic is modelled externally to the amplifier design. Two NMOS are connected to the input and output of the amplifier for filtering. The whole amplifier is then powered through a clock circuit rather than a DC input which can be matched with the heartbeat through the PLC. The clocking circuit is necessary as each clock cycle causes the power to get regenerated. This regenerated power is used in the next cycle causing the whole power requirement in the circuit to decrease in Figure 4.

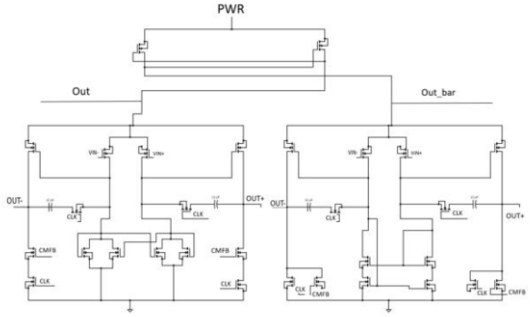

Figure 4 OP-Amp Circuit with Adiabatic Logic

6. Results

The circuit was built and simulated in the software tool Cadence Virtuoso. We utilized the 180nm library to design the circuit in Figure 5.

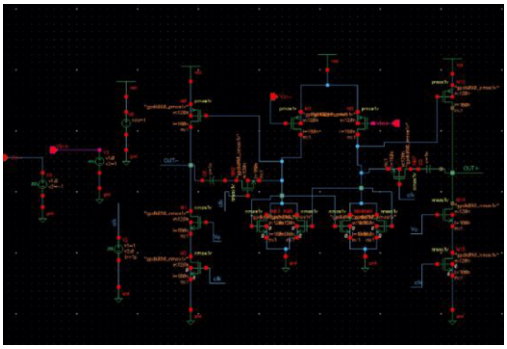

Figure 5. Simulated op-amp circuit

We observed that the original CMOS OP-AMP provided a standard gain in plot when tested in AC analysis. On multiple simulations we observed a power dissipation between 40 to 50 μ W in Figure 6.

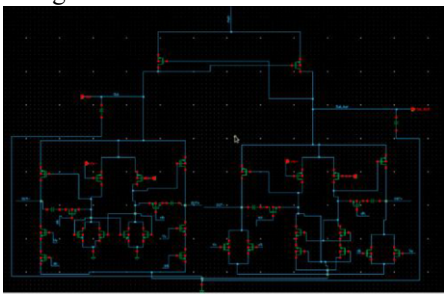

Figure 6. Simulated op-amp circuit with adiabatic logic

The proposed adiabatic circuit was implemented by adding a clocked Vout, there were distortions present in the waveform as the clock changed from high to low and vice versa The power dissipated on simulating using similar conditions as the CMOS OP-AMP yielded in power levels of 30-38hW in Figure 7.

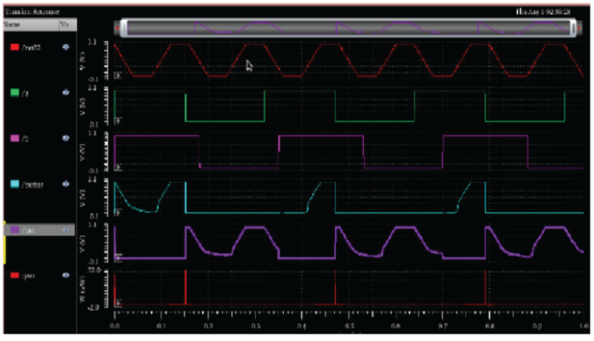

Figure 7. Adiabatic logic output waveforms

Through the simulations, we can observe a power conservation of about 18% when the circuit is implemented using the adiabatic circuit.

7. Conclusion

This project allows the understanding of the impact of adiabatic circuits in modern-day circuitry. This concept can be implemented in critical applications such as pacemakers helping in the increase of the lifespan of the device. Adiabatic Logic is a game-changing domain of VLSI circuit design which reduces the cost of maintenance when applied. The future scope of this project can be the utilization of higher complexity adiabatic logic circuits such as PFAL and ERCL and implementation on a larger scale for a higher level of power conservation. The invention of the pacemaker has contributed to the well-being of millions across the world. This project helps enhance the workings of a pacemaker and better human healthcare.

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