Mechatronics and Automation Technology
J.-Y. Xu (Ed.)

doi:10.3233/ATDE231097

A Novel Half-Bridge Integrated ZVS Full-Bridge DC/DC Converter Based on the Secondary Side Auxiliary Resonant Circuit

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Abstract. In this paper, a novel half-bridge integrated zero-voltage full-bridge soft-switching DC-DC converter based on the secondary auxiliary resonant loop is proposed for medium to high power applications with medium and high voltage output. Compared with the other converters, this converter can eliminate circulation losses and reduce the reverse recovery losses of the rectifier diodes, improving the efficiency of the converter. The overall volume of the converter is reduced and the power density is increased. The principles, circuit characteristics and soft switching conditions of the converter are analyzed in detail. The performance and effectiveness of the circuit are verified by experiments based on a 1.2 kW-50 kHz circuit.

Keywords. Full-bridge DC-DC Converter; Zero-voltage Switching (ZVS); Zero-current Switching (ZCS); Resonance.

1. Introduction

Nowadays, phase-shift full-bridge (PSFB) converters are broadly used in high-power DC-DC conversion occasions such as power supply and electric vehicle on-board batteries because of their simple structure, simple control, low voltage and current stress and high efficiency [1], but traditional ZVS PSFB converters have the following disadvantages: narrow soft switching range, large circulating current loss, rectifier diodes have reverse recovery loss, parasitic oscillations and voltage spikes [2-4].

The ZVS range can be broadened by adding passive auxiliary circuits or active switches [5-8]. However, it brings the problem of having too many components or increasing control complexity and cost. In a half-bridge (HB) integrated full-bridge (FB) converter, a HB converter is integrated into the FB converter by sharing a switch bridge arm. Such converters can expand the ZVS range while reducing the number of components and its current stress, but increasing the losses of the rectifier diodes [9-11]. According to [12,13], the resonance of the secondary side (SR) can be used to realize the ZCS shutdown of the rectifier diodes, eliminate the reverse recovery loss, and improve the efficiency of the converter.

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As shown in figure 1, the novel HB-FB-SR converter based on secondary side resonance adopts an asymmetric control strategy, which can implement the ZVS of the MOSFETs in the full load range and the ZCS of the rectifier diodes, while eliminating the reverse recovery loss of the rectifier diode and eliminating circulating loss, further improving the efficiency and power density of the converter.

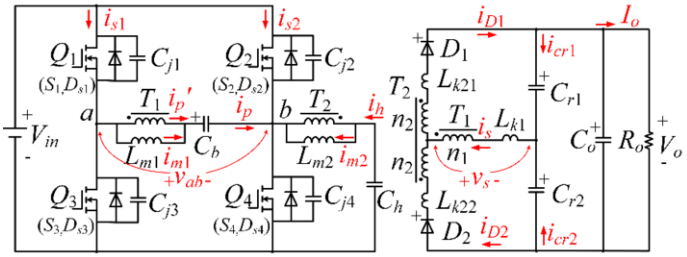

Figure 1. Novel HB-FB-SR DC-DC converter topology.

2. Proposed Converter

2.1. Circuit Configuration

As shown in figure 1, in the proposed converter, Q_1~Q_4, T_1, C_b and D_1, D_2, C_{r1}, C_{r2} form FB converter, Q_2, Q_4, T_2, C_h, D_1, D_2 form HB converter. They are integrated by sharing the Q_2 and Q_4 legs of the switch. To simplify the analysis, the following assumptions apply:

- Switches Q_1~Q_4 are ideal MOSFETs except for the body-diodes D_{s1}~D_{s4} and parasitic capacitance C_{oss}, and $C_{oss} = C_{j1} = C_{j2} = C_{j3} = C_{j4}$.
- The transformers are ideal transformers with the transformation ratio of 1: n, a magnetizing inductance L_m and a secondary side leakage inductance L_k. The leakage inductance of T_1 is L_{k1}, and the leakage inductance of T_2 is $L_{k21} = L_{k22} = L_{k2}$.
- The voltage on blocking capacitor C_b is kept constant to prevent transformer saturation; C_h is large enough to be regarded as a $0.5V_{in}$ voltage source; the resonant capacitors $C_{ro} = C_{r1} = C_{r2}$, and the voltage ripple on them is ignored.

2.2. Principles of Operation

Figure 2 and figure 3 are the key waveform and operating modes plot of the converter, respectively.

In figure 2, V_{gs} is the drive signal waveform of the switch Q_1~Q_4. It can be seen that the converter adopts an asymmetric pulse-width modulation strategy, the switching period is T_s, the duty cycle is d ($d \leq 0.5$), and the dead time between the switch bridge legs is extremely short. There is an extremely short dead time between the switch legs.

The converter has eight *Modes* in a working cycle, and before *Mode* 1 starts, Q_2 and Q_3 are ON.

***Mode* 1 [t_0~t_1]:** Before t_0, Q_2 and Q_3 are ON. At t_0, Q_2 and Q_3 are turned off. C_{j2} and C_{j3} are being charged, C_{j1} and C_{j4} are being discharged. The parasitic capacitances are very small, so the time interval of this mode is short.

***Mode* 2 [t_1~t_2]:** At t_1, the voltage of C_{j1} and C_{j4} reaches zero, D_{s1} and D_{s4} conduct. The converter transfers energy to the secondary side, i_m increases linearly, the rectifier diode D_1 is turned on, L_{k1} and L_{k21} resonant with C_{r1} and C_{r2}. The critical voltage and current for *Mode* 2 can be expressed as

$$i_s(t) = [n_1V_{p1} + 0.5n_2V_{in} - V_{cr1}(t_1)]\, sin[\,\omega_r(t - t_1)]/Z_r \tag{1}$$

$$V_{cr1}(t) = n_1V_{p1} + 0.5n_2V_{in} - [n_1V_{p1} + 0.5n_2V_{in} - V_{cr1}(t_1)]\, cos[\,\omega_r(t - t_1)] \tag{2}$$

$$V_{cr2}(t) = V_o - \{n_1V_{p1} + 0.5n_2V_{in} - [n_1V_{p1} + 0.5n_2V_{in} - V_{cr1}(t_1)]\, cos[\,\omega_r(t - t_1)]\} \tag{3}$$

where,

$$Z_r = \sqrt{(L_{k1} + L_{k2})/2C_{ro}},\ \omega_r = 1/\sqrt{2C_{ro}(L_{k1} + L_{k2})} \tag{4}$$

During this time, Q_1 and Q_4 can achieve ZVS if the driver signal is given before i_p increase to zero.

***Mode* 3 [t_2~t_3]:** At t_2, Q_1 and Q_4 receive the pulse signals, while D_{s1} and D_{s4} are conducting, i.e., Q_1 and Q_4 turn on under ZVS. This interval is the same as *Mode* 2， and it won't end until the switching manager Q_1 and Q_4 received the cutting signal.

***Mode* 4 [t_3~t_4]:** Q_1 and Q_4 turn off at t_3. C_{j1} and C_{j4} are being charged, C_{j2} and C_{j3} are being discharged. This interval is very short, which can be ignored during this period of electricity.

***Mode* 5 [t_4~t_5]:** The voltage of C_{j2} and C_{j3} drop to zero at t_4, D_{s2} and D_{s3} turn on. The converter continues to transfer energy to the secondary side. The leakage current cannot be changed immediately, so D_1 continues to be freewheeling, the secondary current is decreases.

$$\begin{aligned} i_s(t) = {} & [-n_1V_{p2} + 0.5n_2V_{in} - V_{cr1}(t_4)]\, sin[\,\omega_r(t - t_4)]/Z_r \\ & + i_s(t_4)\, cos[\,\omega_r(t - t_4)] \end{aligned} \tag{5}$$

$$\begin{aligned} V_{cr1}(t) = {} & -n_1V_{p1} + 0.5n_2V_{in} + \left[n_1V_{p1} - 0.5n_2V_{in} + V_{cr1}(t_4)\right] \\ & cos[\,\omega_r(t - t_4)] + n_1V_{p1} - 0.5n_2V_{in} - V_{cr1}(t_1)]\, sin(\,\omega_r dT_s)\, sin[\,\omega_r(t - t_4)] \end{aligned} \tag{6}$$

$$\begin{aligned} V_{cr2}(t) = {} & V_o + n_1V_{p1} + 0.5n_2V_{in} - \left[n_1V_{p1} + 0.5n_2V_{in} + V_{cr1}(t_4)\right] \\ & cos[\,\omega_r(t - t_4)] - [n_1V_{p1} + 0.5n_2V_{in} - V_{cr1}(t_1)]\, sin(\,\omega_r dT_s)\, sin[\,\omega_r(t - t_4)] \end{aligned} \tag{7}$$

During this interval, Q_2 and Q_3 can achieve ZVS if the driver signal is given before i_p decrease to zero.

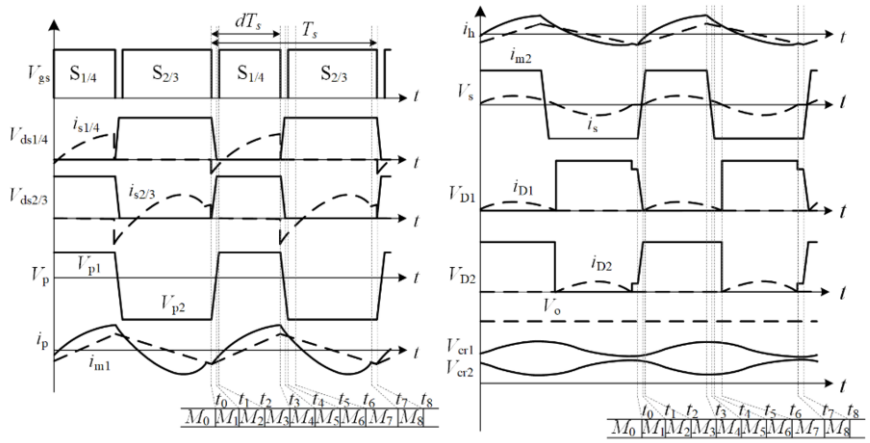

Figure 2. Key waveforms.

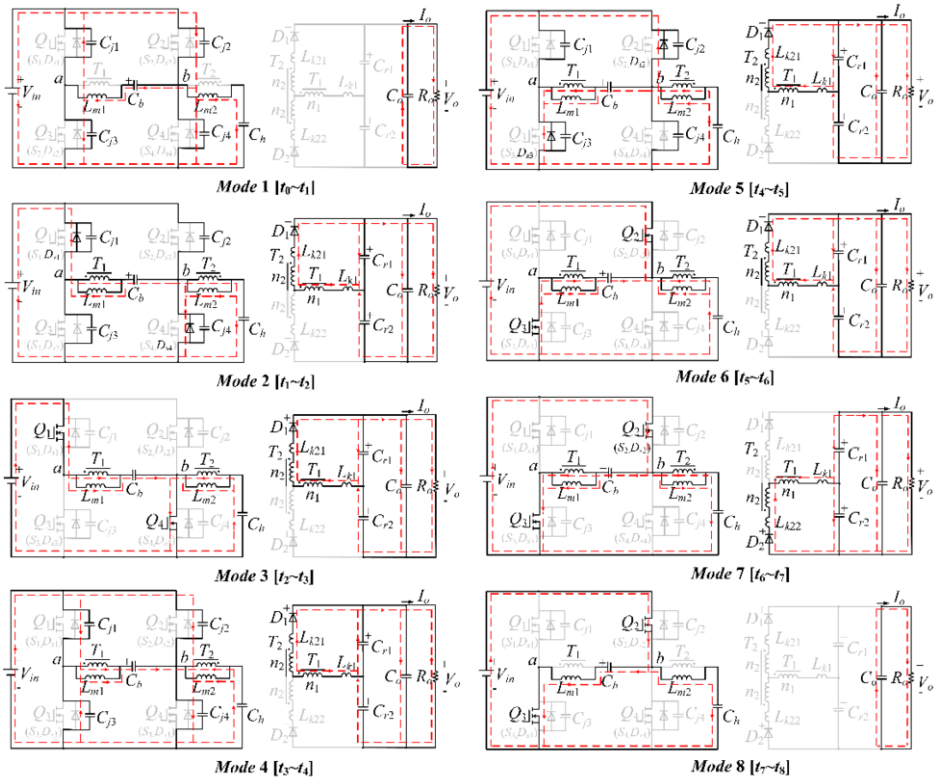

Figure 3. Operational modes.

***Mode* 6 [t_5~t_6]:** At t_5, Q_2 and Q_3 receive pulse signals, while D_{s2} and D_{s3} are conducting, i.e., Q_2 and Q_3 turn on under ZVS. This interval operates the same as *Mode* 5 until the freewheeling current i_{D1} drops to zero.

***Mode* 7 [t_6~t_7]:** At t_6, i_{D1} decrease to zero, and D_1 turns off under ZCS, eliminating reverse recovery losses. At this time, D_2 is turned on, L_{k1} and L_{k22} resonant with C_{r1} and C_{r2}.

$$i_s(t) = [n_1V_{p2}+0.5n_2V_{in} - V_{cr2}(t_6)]\, sin[\,\omega_r(t-t_6)]/Z_r \tag{8}$$

$$V_{cr2}(t) = n_1V_{p2}+0.5n_2V_{in} - [n_1V_{p2} + {}_{0.5}n_2V_{in} - V_{cr2}(t_6)]\, cos[\,\omega_r(t-t_6)] \tag{9}$$

$$V_{cr1}(t) = V_o - \{n_1V_{p2} + {}_{0.5}n_2V_{in} - [n_1V_{p2}+0.5n_2V_{in} - V_{cr2}(t_6)] \\ cos[\,\omega_r(t-t_6)]\} \tag{10}$$

***Mode* 8 [t_7~t_8]:** At t_7, i_{D2} resonates to zero, and D_2 turns off under ZCS, eliminating reverse recovery losses. Q_2 and Q_3 continue to be on, V_{Cr1} and V_{Cr2} remain unchanged, and C_o provides energy for the load. Q_2 and Q_3 are turned off at t_8, the next duty cycle starts.

3. Circuit Characteristics

3.1. Circulating Current Loss

The resonant period of the converter is:

$$T_r = 2\pi\sqrt{2C_{ro}(L_{k1}+L_{k2})} \tag{11}$$

The converter should be operated in the $dT_s \le T_r/2 \le (1-d)T_s$ state. In this range, i_s is sinusoidal, and the period of zero current state in the second half of the cycle is short, the voltage gain is regulated by the duty cycle, the switch turn-off loss is small. It is easy to find that the converter does not have a voltage 0 state, i.e., V_p only changes between +1 and -1 states, and when the primary current exists, the transformer will continuously transmit the primary power to the secondary side, eliminating the circulation loss and improving the efficiency of the converter.

3.2. Voltage Gain

In order to simplify the theoretical analysis, the change of electrical parameter during the charging and discharging of parasitic capacitance of the MOSFETs, the dead time and the voltage ripple is ignored. And then using volt-second balance theorem on T_1 and T_2, the steady-state equations of the proposed converter can be obtained as:

$$V_{p1}dT_s = V_{p2}(1-d)T_s \tag{12}$$

$$kV_{cr1}T_r/2 = ({}_{0.5}n_2V_{in} + n_1V_{p2})(T_s - T_r/2) \tag{13}$$

$$kV_{cr2}T_r/2 + [(1-d)T_s - T_r/2](n_1V_{p2}+0.5n_2V_{in}) = ({}_{0.5}n_2V_{in} + n_1V_{p1})dT_s \tag{14}$$

$$G = V_o/n_1V_{in} = (4+2m)dF \tag{15}$$

where,

$$k = (n_1^2 L_{m1} + n_2^2 L_{m2})/(n_1^2 L_{m1} + n_2^2 L_{m2} + L_{k2}) \tag{16}$$

$$m = n_2/n_1, F = f_r/f_s, F > 1/2 \tag{17}$$

As shown in (15) and figure 4, when F takes the minimum value of 0.5, as long as it is satisfied

$$m < 2d/(1-2d) \tag{18}$$

the voltage gain G of the converter mentioned in this article can be higher than that of [11].

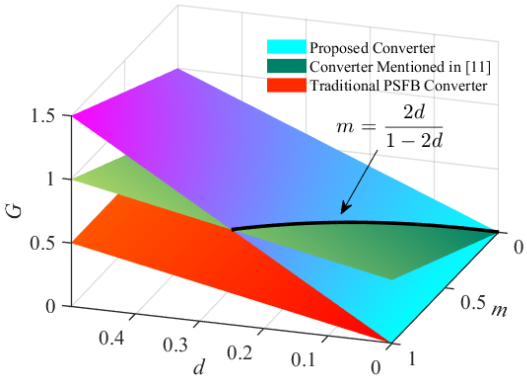

Figure 4. Converter voltage gain curve.

3.3. Soft Switching Conditions

Q_1 and Q_4 are more difficult to achieve soft switching than Q_2 and Q_3, so when Q_1 and Q_4 meet ZVS, Q_2 and Q_3 can also achieve soft switching. When Q_1, Q_4 implement soft switching, i_{m1} and i_{m2} need to draw all charge from C_{j1} and C_{j4} within the dead time t_{dead} and charge C_{j2} and C_{j3} of Q_2 and Q_3.

$$|i_{m1}(t_8) + i_{m2}(t_8)| > 2C_{oss}V_{in}/t_{dead} \tag{19}$$

In order to ensure the ZCS of the rectifier diode, the current flowing through it needs to be reduced to zero after Q is switched on and off, that is, half of the resonance period needs to be greater than the on-time of Q_1 and Q_4, and less than the on-time of Q_2 and Q_3 ($d \leq 0.5$).

$$\pi/\omega_r < dT_s,\ \pi/\omega_r > (1-d)T_s \tag{20}$$

From (19) and (20), the soft switching conditions of the converter can be obtained as

$$L_{m1}L_{m2}/(0.5L_{m1} + 2dL_{m2}) < (1-d)T_s t_{dead}/2C_{oss} \quad (21)$$

$$d^2/2\pi^2 f_s^2(L_{k1} + L_{k2}) < C_{ro} < (1-d)^2/2\pi^2 f_s^2(L_{k1} + L_{k2}) \quad (22)$$

From (21), we can see that the ZVS condition is independent of output current I_o, the converter can achieve ZVS in the full load range.

4. Experimental Results

This section uses experiments to prove the performance of the circuit, and the parameters are set as follows: f_s = 50 kHz, P_o = 1.2 kW, V_{in} = 260 V, V_o = 60 V. The parameters of the other major components and their parameters are detailed in table 1.

Table 1. Components And Parameter.

Component	Parameter		
	Model	**Parameter Value**	**Volume(*Number)**
Switch Q_1~Q_4	IPB407N30N	300 V, 44 A	0.35 cm^3(*4)
Rectifier Diodes D_1, D_2	MBR6035PT	100 V, 60 A	1.62 cm^3(*2)
T_1 Core (Turns Ratio, L_{m1}, L_{k1})	PC95PQ35/35Z-12	0.08, 1 mH, 0.8 μH	34.60 cm^3
T_2 Core (Turns Ratio, L_{m2}, L_{k2})	PC95PQ35/35Z-12	0.08, 150 μH, 0.6 μH	24.00 cm^3
Blocking Capacitor C_b	L1GN30D334KA04	0.3 μF	2.07 cm^3
Clamping Capacitor C_h	MLP561M300EB1A	10 μF	7.21 cm^3
Resonant Capacitor C_{r1}, C_{r2}	L22E405JV1	4 μF	5.5 cm^3(*2)
Output capacitor C_o	80ZLJ470M13X30	470 μF	3.68 cm^3

Figure 5 shows the measured waveforms of the converter at the rated load for this parameter. From figure 5a–d, we can see the MOSFETs implement ZVS and the rectifier diodes turn off under ZCS.

Figure 6a shows the comparison of the losses of different converters at rated load. It can be seen that under the rated load, the switching loss of the proposed converter is 5.72 W, the transformer loss is 6.20 W, and the rectifier diodes loss is 16.58 W without reverse recovery loss. Figure 6b shows the efficiency curves of the three converters at different loads conditions under the same experimental environment and parameters. Under the rated load, the theoretical calculation efficiency of the converter is 97.63%,
which is basically consistent with the experiment shown in figure 6b. The proposed converter eliminates the circulation loss, so the efficiency improvement is more significant under light load conditions. Since the reverse recovery loss of the rectifier diodes hardly changes with the load, the proportion of this part of the loss will increase with the decrease of the load, and the rectifier diodes of the proposed converter turn off under ZCS, which solves the reverse recovery problem. Therefore, compare with the traditional PSFB converter and the converter mentioned in [11], the proposed converter can maintain higher efficiency over the full load range.

Besides, the total volume of the converter is small, which allows higher power densities to be obtained.

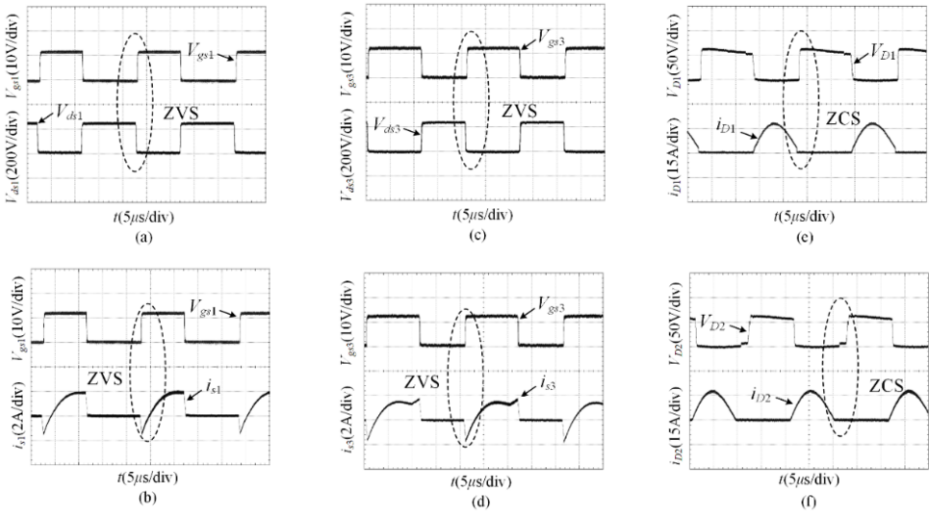

Figure 5. Measured waveforms of the converter.

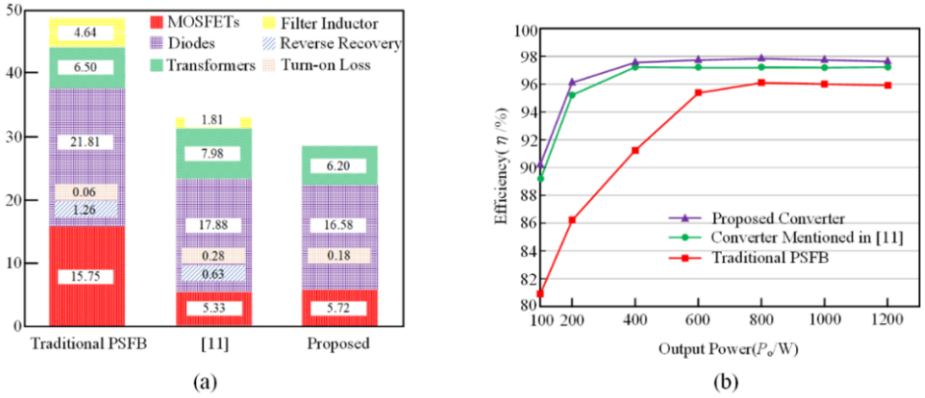

Figure 6. Converter losses comparison and efficiency curve.

5. Conclusion

A novel HB-FB-SR converter topology based on secondary side resonance is proposed in this paper. It has the following advantages: (1) MOSFETs implement ZVS over the full load range, (2) an asymmetric PWM strategy is used to eliminate the circulation loss of the converter, (3) the rectifier diodes reduce reverse recovery losses by turning off under ZCS, while improving converter efficiency. Besides, the overall volume of the converter is reduced and the power density is increased. The operating principle and characteristics of the converter are discussed. Finally, the correctness of the theoretical analysis is verified by experiments.

References

[1] Zhang T. The design of full bridge EV charger based on LLC[J]. Electrical Engineering, 2018, 19 (08): 164–167 (in Chinese).

[2] Xie J, Ma J, Ji Y, Zhang Z and Wu Q. Topology study of phase-shifted full-bridge converter[J]. Technology Innovation and Application, 2021, 11 (32), 51-54 (in Chinese).

[3] Braun W D, Stolt E A, Gu L and Rivas-Davila J M. Reverse Recovery Testing of Small-Signal Schottky Diodes[C]. 2021 IEEE Energy Conversion Congress and Exposition (ECCE), Vancouver, BC, Canada, 2021, pp. 5611-5615.

[4] Ruan X. Pulse width modulated DC/DC full bridge soft switching technique[M]. Beijing: Science Press, 2012, 29–39 (in Chinese).

[5] Moisseev S, Ishigami Y, Soshin K and Nakaoka M. Tapped-inductor filter assisted soft-switching PWM DC–DC power converter[J]. IEEE Transactions on Aerospace and Electronic Systems, 2005, 41 (1): 174–180.

[6] Kim E -S and Kim Y -H. A ZVZCS PWM FB DC/DC converter using a modified energy-recovery snubber[J]. IEEE Transactions on Industrial Electronics, 2002, 49 (5): 1120–1127.

[7] Tran D -D, Vu H -N, Yu S and Choi W. A Novel Soft-Switching Full-Bridge Converter with a Combination of a Secondary Switch and a Nondissipative Snubber[J]. IEEE Transactions on Power Electronics, 2018, 33 (2): 1440–1452.

[8] Pan X, Li H, Liu Y, Zhao T, Ju C and Rathore A K. An Overview and Comprehensive Comparative Evaluation of Current-Fed-Isolated-Bidirectional DC/DC Converter[J]. IEEE Transactions on Power Electronics, 2020, 35 (3): 2737-2763.

[9] Gu B, Lin C -Y, Chen B, Dominic J and Lai J -S. Zero-Voltage-Switching PWM Resonant Full-Bridge Converter with Minimized Circulating Losses and Minimal Voltage Stresses of Bridge Rectifiers for Electric Vehicle Battery Chargers[J]. IEEE Transactions on Power Electronics, 2013, 28 (10): 4657-4667.

[10] Lim C -Y, Jeong Y, Lee M -S, Yi K -H and Moon G -W. Half-Bridge Integrated Phase-Shifted Full-Bridge Converter with High Efficiency Using Center-Tapped Clamp Circuit for Battery Charging Systems in Electric Vehicles[J]. IEEE Transactions on Power Electronics, 2020, 35 (5): 4934-4945.

[11] Chen J, Liu C, Liu H and Li G. Zero-Voltage Switching Full-Bridge Converter with Reduced Filter Requirement and Wide ZVS Range for Variable Output Application[J]. IEEE Transactions on Industrial Electronics, 2022, 69 (7): 6805-6816.

[12] Chen J J and Lin B R. Analysis of ZVS/ZCS soft-switching dual-resonant converter[C]. 2009 International Conference on Power Electronics and Drive Systems (PEDS), Taipei, Taiwan, 2009, pp. 411–416.

[13] Wang H and Li Z. A PWM LLC Type Resonant Converter Adapted to Wide Output Range in PEV Charging Applications[J]. IEEE Transactions on Power Electronics, 2018, 33 (5), 3791-3801.