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Design of FinFET Based Op-Amp Using High-K Device 22 nm Technology

Vasudeva G[a1], Mandar JATKAR[a], Tripti R KULKARNI[a], Roopa R KULKARNi[a], Bharathi GURURAJ[b] and Tejas M P[a]
[a] *Department of Electronics and Communication Engineering, Dayananda Sagar Academy of Technology and Management, Bangalore (560082), Karnataka, India*
[b] *Department of Electronics and Communication Engineering, ACS College of Engineering, Bangalore (560060), Karnataka, India*

Abstract. In this research paper, a design for circuit of an operational amplifier (OP-AMP) is formulated utilizing model characteristics of FinFET using high -k gain in the context of 22 nm technological advancements.To create an OP-AMP based on FinFET technology, the standard design equations for MOSFET-based OP-AMP design are tuned to FinFET based OPAMP. The OP-AMP architecture is well-suited for implementation as a subordinate circuit in the ADC design since it supports lower voltage, elevated velocity, and diminished power dissipation.. The geometries of the transistors are organised to accomplish an OP-AMP that exhibits superior fulfilment and energy efficiency.Using cadence tool schematic is captured.Results show that the developed OPAMP exhibits a UGB of 100 GHz based on simulation experiments and a slew rate below 10V/µS. The inverter circuit amounts to power dissipation of 800nW, thereby rendering it suitable for a wide range of low-power analog and digital circuits.

Keywords. Fin-FET; differential amplifier; OP-AMP; HIGH-K; DG-FET.

1. Introduction

It is impossible to overestimate the importance of high-performance Analog_to_ Digital_Converters (ADCs) in signal-processing applications, as they serve as the vital interface between sensors acquiring real-world signals and digital signal processors responsible for processing these signals in the digital domain. SAR, or the Successive Approximation Register, is one of the many types of ADCs that are employed in signal processing because of its significant advantages in terms of power dissipation. With approximately 50% of their circuit topology comprising digital components, SAR ADCs are preferred choices. It is worth noting that SAR logic necessitates a greater number of steps to determine the corresponding pattern of digital for each analog input, resulting in longer conversion time compared to flash ADCs, which accomplish the conversion more swiftly Asynchronous ADC architecture presented by S. Hsieh et al. [1] aims to shorten conversion time by removing the clock from the SAR logic. Nevertheless, despite the

[1] Corresponding Author, Vasudeva G, Department of Electronics and Communication Engineering, Dayananda Sagar Academy of Technology and Management, Bangalore (560082), Karnataka, India ; E-mail: vasudeva-ece@dsatm.edu.in.

utilization of different reset operations of comparators at each step, the improvement in conversion time remains limited [2,3]. have presented high-resolution ADCs operating at 150 MS/s with low power dissipation [4]. showcases time-interleaved and pipelined ADCs with SAR logic, showcasing both high-speed operation and high resolution [5]. have created an asynchronous pipelined SAR ADC using 28 nm CMOS technology that operates at MSPS with a power dissipation of less than 3.5 mW. However, due to the two-stage pipeline operation, the main drawbacks of this design are power dissipation and die area. Although the SAR-based ADC is thought to be capable of obtaining high resolution, its slower speed is caused by the SAR logic, literature offers several approaches for SAR ADC design, focusing on achieving high resolution, low power consumption. The efficiency of ADCs has shown improvement through scaling of MOS transistor dimensions and power supply [6]. Analog circuits' Signal to Noise Ratio (SNR) has been found to deteriorate as the power supply voltage is reduced [7]. Subthreshold operation of CMOS technologies has been adopted in ADC architecture to increase energy sufficiency, considering the trade-off among speed, noise performance, and area requirements [8]. However, the energy efficiency of CMOS-based ADCs, especially in low-resolution ADCs, is limited. Challenges such as current leakage and device-to-device variation significantly impact CMOS technology of sub-22 nm. To reduce energy consumption, it becomes vital to investigate alternatives to MOS transistors [9]. It has been determined that Multi Gate FETs (MG-FETs) or Double Gate FETs (DG-FETs) are promising options to address these issues. MG-FETs, particularly in DGFETs, feature a narrow channel width and multiple gate on both sides of the contact channel, effectively controlling current flow. MG-FETs not only minimize short channel effects but also offer improved control over the active channel through the gate electrode, while maintaining compatibility with conventional planar technology of CMOS. This study focuses on the development of an OP-AMP using FIN-FET technology, specifically for the development of high-resolution, high-speed, and low-power ADCs using SAR logic in the context of 22 nm technology. DG-FETs exhibit twice the capability of drive current compared to MOSFETs, enabling operation at low input and sub-threshold voltages, thereby resulting in significantly reduced power dissipation [11,12]. FIN-FET devices have found successful application in the design of digital-to-analog (DA) circuits, emphasizing the need to consider FIN-FETs as the fundamental device in OP-AMP design. Descriptive analysis of the FIN-FET model, as presented in [13], is illustrated in figure 12. The design process for MOSFET-based OP-AMPs is thoroughly covered by Allen Hollberg [14]. The FinFET transistor geometries required for the OP-AMP circuit schematic are discovered using a redesigned and enhanced design process in this work.The design process for FIN-FET-based OP-AMP design is succinctly summarized . Existing literature [15], shows how to use 32 nm technology with a supply voltage of 1 V, 58 W of power usage, a DC gain of 52 dB, and a unity gain frequency of 6.4 MHz and a seventy one degree phase margin. The operational amplifier (OP-AMP) is a crucial component in data converters, and two circuit topologies are commonly employed: the two-stage topology and the folded cascode topology [16]. The two-stage topology represents the simplest form of OP-AMP and provides gain in two stages. The first stage comprises a differential amplifier using two common-source amplifiers and PMOS current mirrors, followed by a common-source amplifier as the second stage [17]. The common-drain amplifier, the third stage of the OP-AMP, bypasses the common-source amplifier by connecting the differential amplifier's output to the common-drain amplifier's input via a bypass capacitance. When operating with a capacitive load at the output, the common-drain amplifier can be eliminated, resulting in

a two-stage OP-AMP [18]. Differential amplifiers (D_A) are incorporated into the OP-AMP's input stage to increase gain, improve noise performance, and improve offset characteristic. To create an OP-AMP that satisfies the necessary specifications, transistor geometries must be systematically determined at each stage and sub-circuit [19,20]. In order to accomplish the CMOS scaling, various nano two-dimensional (2-D) material based devices have been seen to be potential candidates and are useful in nanoscale device applications [21,22].

Table 1. FIN-FET Characteristics.

Parameters	**Value**
Channel width	40 nm
Oxide-level-thickness I	2.5 nm
Oxide-level-thickness II	2.5 nm
Gate length	22 nm
Source/drain length extension	50 nm
Gate-Source/Gate overlaping	2 nm

The input and output characteristics for the FinFET when taken into account with the structural parameters listed in table 1 . By setting the drain voltage between 0.5 and 1 volts, the output is achieved. Also, by Setting the gate voltage between 0 V and 1 V with an incremental step of 0.1 V yields the output characteristic.

The VI properties of FIN-FETs studied at a 22 nm technology with high-K dielectric are shown in Figure 1.

Figure 2 presents gate voltage versus drain current input characteristics with constant output voltage.

Figure 4a explains the FinFET-based inverter's power dissipation and transfer characteristic. With less than 800 nW of maximum power dissipation and 0.12 V of transition width are detected.

Positive switching and negative switching current are discovered to have leakage currents smaller than 9 μA.

The fundamental distinction between a DA and an operational amplifier is that the DA does not require compensation for closed loop feedback because stability is not required [23]. Because of this, there is no longer a requirement for the internal capacitor, which increases the output slew rate. Voltage gain, slew rate, and an offset voltage for a specific over drive are characteristics of D_A [24]. Over drive describes how much differential voltage is present at the input pins, and it typically has a considerable impact on reaction time [25]. When the input thresholds are crossed in typical A/D converter applications, the D_A, which also serves as a comparator, must slew its output rapidly and without oscillation. By providing a step input signal and timing how long it takes the D_A to reach the final output value, the slew rate of the D_A or comparator can be determined [26]. The M1 and M2 transistor geometries are set to 100 nm, the M3 and M4 transistor geometries to 200 nm, the M5 and M8 transistor geometries to 400 nm, and the transistor geometries to handle a maximum driving current of 100 μA .

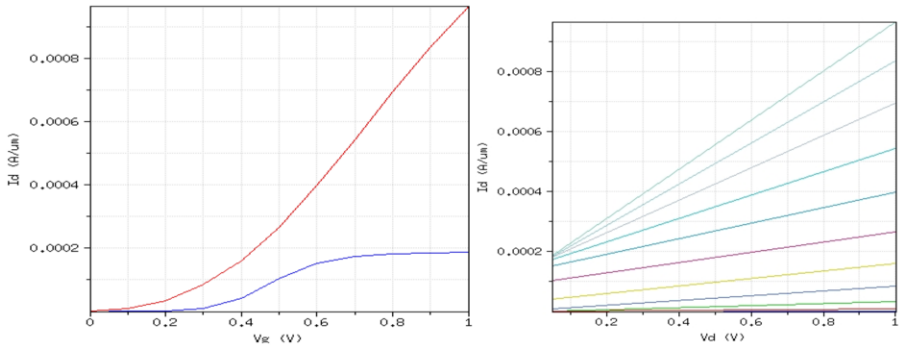


Figure 1. FIN-FET characteristics.

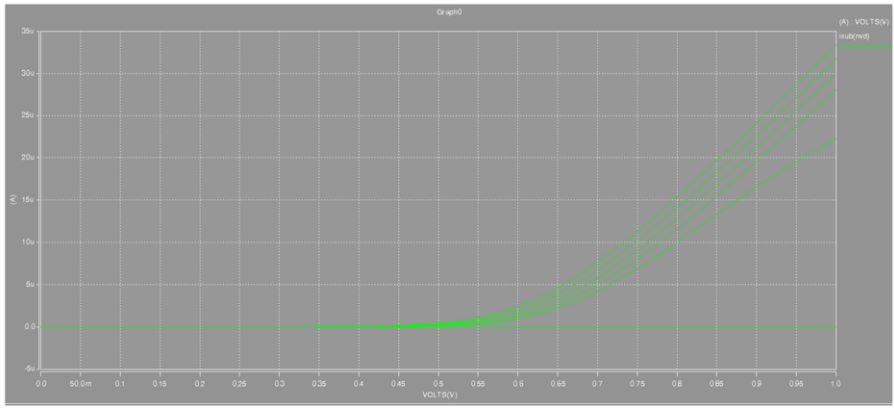


Figure 2. VGS versus IDS input characteristics with constant VDS.

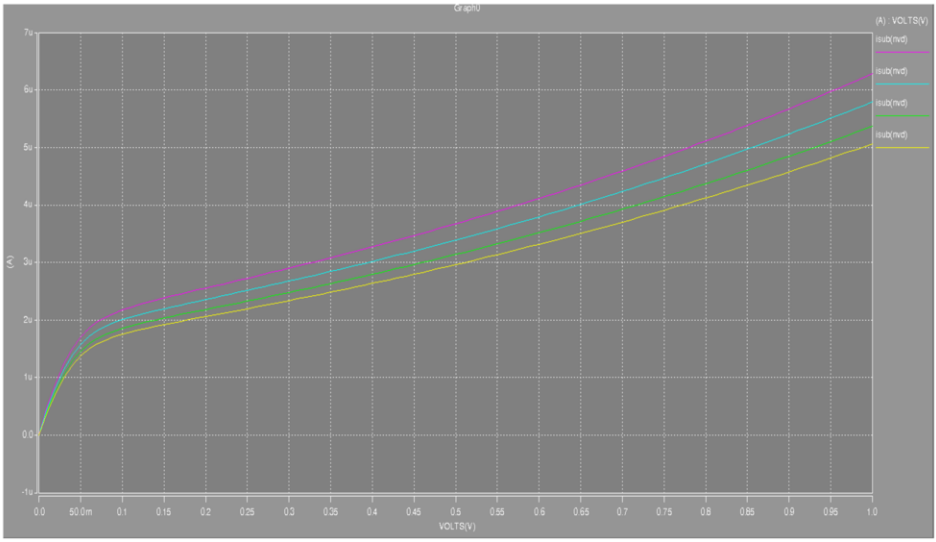
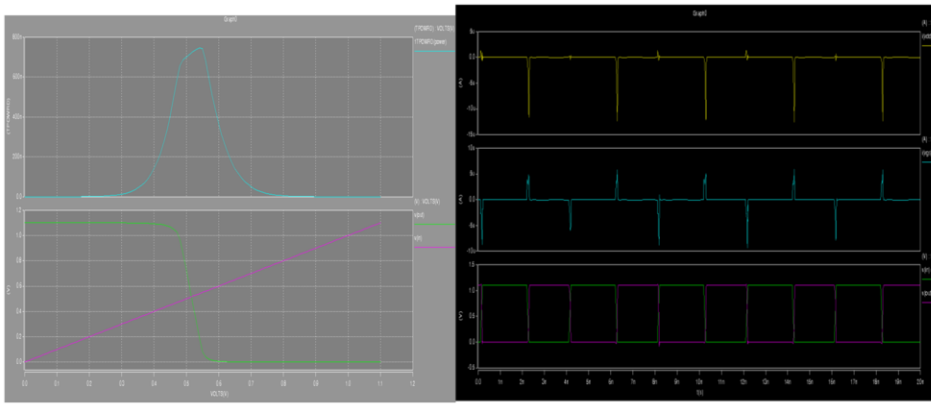


Figure 3. High-k FIN-FET 22 nm output characteristics for variable width.



(a) (b)

Figure 4. (a) Inverter transfer characteristics and Power dissipation; (b) Plot of leakage current with 800nW power dissipation and 0.12V transistor width.

The (D_A) simulation entails a case of test where a piece-wise linear (PWL) signal is utilized as the analog input. 1.8V the power supply is set, and a clock operating at 80 Megha Hertz is employed. To compensate for layout parasitic capacitance-induced clock delay, a 0.3 ns delay is introduced. During the offset cancellation cycle, the comparator runs in closed-loop mode. Hence, phase margin and gain simulations are performed using the ELDO simulator. The expected gain of the Differential Amplifier ranges from approximately 120 to 300 dB, although the gain really attained is about 180 dB. The Differential Amplifier's stability is influenced by the Phase Noise Margin (PNM), with the optimal PNM often ranging between 45° and 75°. The achieved Phase Margin measures 62°. To assess the PSRR, a 1 V AC signal is added, causing the D_A to exhibit a full-scale output when all analog inputs are transitioned from low to high. The D_A's analog output is then analyzed to determine the power supply rejection. The result of the waveform, simulated across various corners, is illustrated in figure 5.

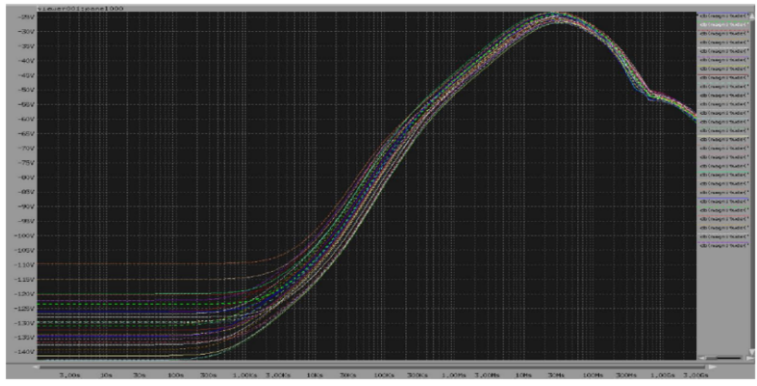


Figure 5. Power supply rejection ratio.

The Power Supply Rejection Ratio (PSRR) is expected to be approximately 45 dB, and it shouldn't go above 45 dB. About 52 dB are measured by the PSRR that was attained.

2. OP-AMP Design

The D_A circuit has demonstrated successful utilization of the FIN-FET device. Consequently, the implementation of FIN-FET as the core component must be considered during OP-AMP design. The threshold voltage of the FIN-FET is given as 0.25 V, while the subthreshold_slope (S_S) stands at 65 mV/dec. The parameters gds and gm, VDS and VGS are measured at 8.97 S/m and 0.18 mS/m, respectively, when it is set to 0.3 V [25]. The on_current and off_current values at I_DS = 10 A/m are 6.20 A/m and 3.3 nA/m, respectively, and the ratio of g_m to IDS is 27/V [26]. With noise power of 1.15e-13 Hz-1 and an operating frequency of 10GHz with V_GS = 0.3V, the FIN-FET has a max operational frequency of 140 GHz. The two-stage OP-AMP is created by using these model parameters from the technology and model files. Circuit diagram for the two-stage OP-AMP implemented with FIN-FETs is shown in figure 6.

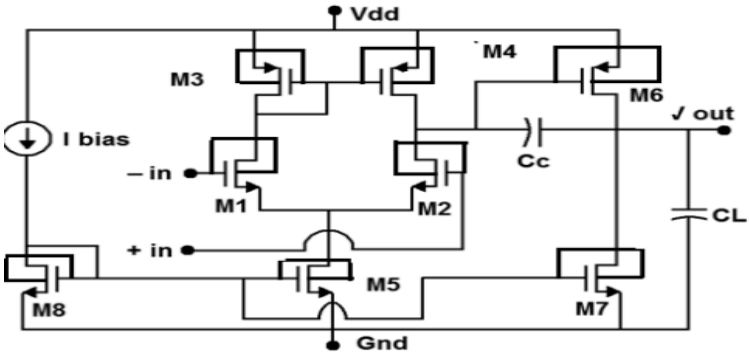


Figure 6. FinFET based OP-AMP [10].

The OP-AMP design requirements taken into account for the SAR ADC design are shown in table 2. With mobility variables taken into account from the model file and the slew_rate is given as larger than 10 V/uS and power dissipation set to lesser than 10 uW, the constants K'n and K'pare computed.

Table 2. OP-AMPs Design-Specifications.

Specifications	Value
Slew-Rate(SR)	>1V/μS
V_{out} range	±1.5Volt
ICM Ratio	0.15-1.2Volt
Power Dissipation	≤ 10μWatt
$V_{tha} = \|V_{tp}\|$	0.25-0.45Volt
$K'_{pa} = \mu_{pa}C_{ox}/2$	-455 μA/Volt²
$K'_{na} = \mu_{na}C_{ox}/2$	1085 μA/Volt²

Allen Hollberg [14] provides details about the design for a MOSFET-based OP-AMP. The design process for an OP-AMP using FIN-FET is summarized in table 3.

Table 3. OP-AMP design procedure process.

Requirement	Expression for MOSFET based OPAMP design [133]	Tuning required for FinFET design
Meeting compensation capacitor from the load capacitor for a 60° phase shift Bias current is calculated using slew rate and compensation capacitor	$I_5 = SR \cdot C_e$ $I_5 \cong 10\left(\frac{V_{DD} + \lvert V_{SS}\rvert}{2 \cdot T_s}\right)$	Similar to MOSFET
Calculating M3 transistor sizing from the ICMR specifications	$S_3 = \frac{I_5}{K_3'\left[V_{DD} - V_{in}(\max) - \lvert T_{T03}(\max) + V_{T1}(\min)\rvert\right]^2} \geq 1$	Similar to MOSFET
Transconductance of the S_1 transistor is calculated from the gain bandwidth specification	$\frac{g_{m3}}{2C_{gs3}} > 10 \text{ GB}$	Limits set to 140GB
Calculating S_1 transistor sizing from the Transconductance	$g_{m1} = GB \cdot C_c \Rightarrow S_2 = \frac{g_{m2}}{K_2' I_5}$	Use model file parameters for mobility
Calculating V_{DS} of transistor S_5 from ICMR specification	$V_{DS5}(\text{sat}) = V_{in}(\min) - V_{SS} - \sqrt{\frac{I_5}{\beta_1}} - V_{T1}(\max) \geq 100 \text{ mV}$ $S_5 = \frac{2I_5}{K_5'\left[V_{DS5}(\text{sat})\right]^2}$	Set upper threshold to 100 mV and use mobility constant from model file
Finding transconductance of S_6 from g_{m1}	$g_{m6} = 2.2 g_{m2}\left(C_L / C_c\right)$ $S_6 = S_3\left(\frac{g_{m6}}{g_{m3}}\right)$	Similar to MOSFET
Finding S_6 transistor sizing from the Transconductance of g_{m6} and g_{m4}	$I_6 = \left(S_6 / S_4\right) I_4 = \left(S_6 / S_4\right)\left(I_5 / 2\right)$	Similar to MOSFET

Calculating I_6	$I_6 = (g_{m6})^2/2\ K'_6(W/L)_6$	Use model file parameters for mobility
Finding S_7 from the S_5, I_6 and I_5	$(W/L)_7 = (W/L)_5 * I_6 / I_5$	Similar to MOSFET
Finding $V_{min}(out)$ considering W7	$V_{min}(out) = V_{DS7(sat)} = \frac{\sqrt{2 \cdot I_6}}{K'(W/L)_7}$	Use model file parameters for mobility
Calculating the power dissipation of OPAMP Verification of the gain of two-stage operational amplifier	$A_v = \frac{2g_{m2}g_{m6}}{I_5(\lambda_2 + \lambda_3)I_6(\lambda_6 + \lambda_7)}$ $P_{diss} = (I_5 + I_6)(V_{DD} + \lvert V_{SS} \rvert)$	Lambda is approximately zero in FinFET (assumed to be very less number)

The performance of FIN_FET is evident in its ability to carry high currents, as a mere 0.1V change in gate voltage results in a 200 µA increase in drain current. This characteristic highlights the significance of determining appropriate transistor dimensions for the building of high-performance OP-AMPs that prioritize low power and high-speed consumption. Equation (1) expresses the variation of gm/IDS for FIN-FET in relation to VGS, taking into account the steep_slope (S_S) necessary to conquer the constaint of CMOS, which typically reaches 40 V-1 [29]. It should be noted that increasing g_m/I_DS could lead to higher power dissipation in FIN-FET, which could be regulated by decreasing V_DD in circuit designs. When designing CMOS-based OP-AMPs, a trade-off between gm/IDS and fT = (g_m/2(C_gs+ C_gd)) must be considered. However, in FIN-FET-based OP-AMP designs, a higher gm/IDS can be achieved without compromising the desired maximum fT requirement [30]. This characteristic enables energy savings through lower VDD in FIN-FET-based OP-AMP designs, without impacting the maximum frequency, drive strength, and operational bandwidth [31]. As a result, the OP-AMP becomes a suitable foundational component for SAR ADC designs [32].

$$\frac{\partial I_{DS}}{\partial V_{GS}}\left[\frac{1}{I_{DS}}\right] = \frac{g_{m,FINFET}}{I_{DS}} = \frac{\partial \ln I_{DS}}{\partial V_{GS}} = \frac{\ln 10}{SS} \tag{1}$$

The aforementioned equation elucidates the relationship between transconductance (gm) and Drain-to-Source Current (IDS) in the context of FIN-FET. In FIN-FET, the absence of channel doping results in higher effective mobility, leading to increased gm [33]. Furthermore, the channel length modulation factor (λ_c) is significantly reduced in FIN-FET. This reduction in λ enhances the gain factor in OP-AMP designs, as outlined in table 3. To compensate for this effect, the current flowing through transistors M5 and

M6 is reduced, thereby halving the transistor width compared to MOSFET transistor designs [34]. The transistor dimensions for the OP-AMP design are investigated and summarized in table 4.

Table 4. Transistor design using MOSFET and FIN-FET technology.

Transistor number	W(nM) MOSFET design	W (nM) FIN-FET design
M_1	200	100
M_2	200	100
M_3	1200	600
M_4	1200	600
M_5	800	400
M_6	1600	800
M_7	1400	700
M_8	800	400

3. Results & Discussion

The OP-AMP circuit implementation is done using 22 nm high-k FIN-FET technology and realized using cadence. The SPICE code simulations are conducted using the HSPICE simulator. The FIN-FET model device configuration are obtained from an online simulator on nanohub.org. Using PTM model files, the electric tool is configured for validation of device models. The results for AC and DC analysis is obtained using cadence environment. Common Mode Rejection Ratio (CM_RR), Power Supply Rejection Ratio (PS_RR) and output voltage range are measured. In order to determine the frequency response of the designed OP-AMP phase margin and gain margin are determined. The simulation results yields a phase margin of 58 degrees and the design criteria was set to achieve a phase margin of 60 degrees. The unity-gain bandwidth (UGB), obtained from the response plot, is measured to be 100 GHz, highlighting the wide operational capability for OP-AMP design.

The input signal without any rise time delay, exhibits a rise time of lesser than 1.2 ns for the output, and a overshoot of lesser than 4%. These results meet the desired specifications, designing the OP-AMP suitable for high-speed applications. Figure 7 illustrates the measurement of the OP-AMP's slew rate by giving the load capacitance as 0.3 pF. The slew_rate is determined as 1 V/μS.

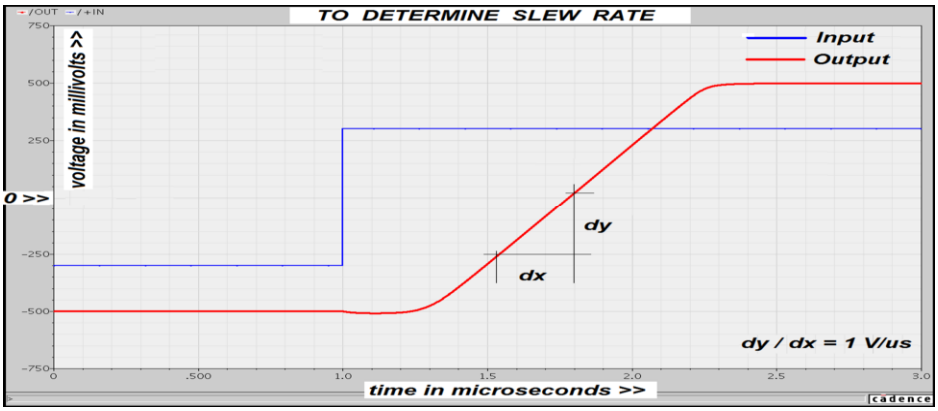


Figure 7. Computing slew_rate of OP-AMP.

Figure 8 depicts the comparator model circuit of OP-AMP by giving DC_voltage as 0 V. The comparator output switches between +/− Voltage rails demonstrating functionality.

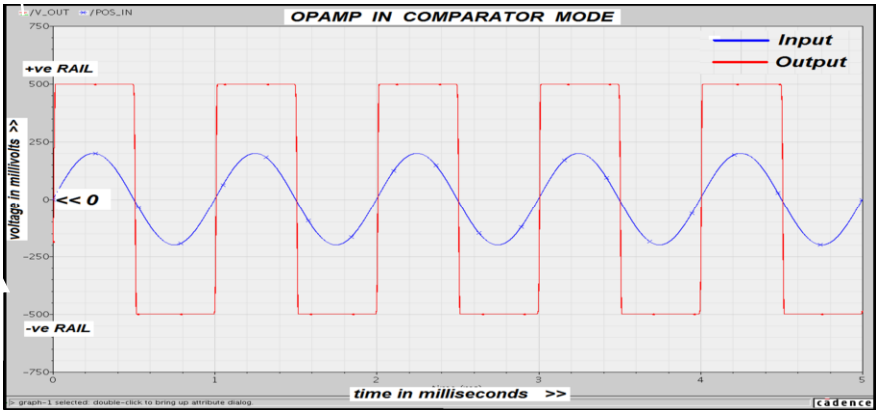


Figure 8. OP-AMP arranged as comparator.

3.1. Comparison

Table 5. Comparison matrix table for OP-AMP with existing technology.[15]

OP-AMP design specification	Previous FIN-FET technology node 32 nm [15]	Proposed work FIN-FET technology node 22 nm	Improvement (%)
PS_RR	32.4 dB	45 dB	28%
UGB	6.4 MHz	100 GHz	99.99%
SLEW_RATE	26.36 V/µS	1 V/µS	96.2%

4. Conclusions

This study presents the design of an OP-AMP circuit for the development of a high-resolution, high-speed, and low-power ADC based on SAR logic. The model parameters

for the high-k FIN_FET model under 22 nm nodes are obtained through PTM. The I-V results of FIN_FET model are plotted, considering the 22 nm node with a high-k dielectric. The output characteristics and inverter properties of the 22 nm high-k FIN_FET-based circuit are designed and found to meet the required specifications. The differential amplifier exhibits a gain greater than 50 dB and a phase margin of 58°.

Previous literature reports using 32 nm technology with 1V supply voltage demonstrated a dc gain of 52 dB, a unity gain frequency of 6.4MHz, and a phase margin of 71°. In this work, a 1 V supply voltage is used, resulting in a 800 nw power dissipation for the inverter circuit. The overall performance of the OP-AMP circuit is gained by 4%. The PS_RR is evaluated at approximately 45 dB. The OP-AMP gains a UGB of 100 GHz, a slew_rate of 1 V/μs, and an over_shoot of lesser than 4%. The OP-AMP is verified by taking the responses of the inverting, non-inverting, and comparator configurations.

References

[1] Hsieh S, Kao C, Hsieh C. A 0.5-V 12-bit SAR ADC Using Adaptive Time-Domain Comparator with Noise Optimization [J]. IEEE Journal of Solid-State Circuits, 2018, 53(10): 2763-2771.

[2] Chen Y, Tsukamoto S, and Kuroda T A 9b 100 MS/s 1.46 mW SAR ADC in 65 nm CMOS [C]. Proc. ASSCC, 2009, 145-148.

[3] Yoshioka M, Ishikawa M, Takayama T, and Tsukamoto S. A 10b 50 MS/s 820 uW SAR ADC with on-chip digital calibration [C]. ISSCC Dig. Tech Papers, 2010: pp. 384-385.

[4] Choi H, Kim Y, Ahn G, and Lee S A 1.2-V 12- b 120-MS/s SHA-free dual-channel Nyquist ADC based on midcode calibration [J]. IEEE Trans. Circuits Syst. I, 2009, 6(5): 894-901.

[5] Tai-ji An, Young-Sea Cho, Jun-Sang Park, Gil-Cho Ahn, and Seung-Hoon Lee. A Two-channel 10b 160 MS/s 28 nm CMOS Asynchronous Pipelined-SAR ADC with Low Channel Mismatch [J]. Journal of Semiconductor Technology And Science, 2017, 17(5).

[6] Murmann B. A/D converter trends: Power dissipation, scaling and digitally assisted architectures [C]. Proc. IEEE Custom Integr. Circuits Conf. (CICC), 2008: pp. 105–112.

[7] Baschirotto A, Chironi V, Cocciolo G, Amico S D, De Matteis M, and Delizia P. Low power analog design in scaled technologies [C]. Proc. Topical Workshop Electron. Particle Phys., Paris, France, 2009: pp. 103–110.

[8] Chen C Y, Wu J, . Hung J, Li T, Liu W, Shih W T. A 12-bit 3 GS/s pipeline ADC with 0.4 mm^2 and 500 mw in 40 nm digital CMOS [J]. IEEE J. Solid-State Circuits, 2012, 47(4): 1013–1021, Apr. 2012

[9] Murmann B. ADC Performance Survey 1997-2013. 2013. [Online] Available: http://http://web.stanford.edu/~murmann/adcsurvey.html

[10] Tosaka Y, Suzuki K, Horie H, Sugii T. Scaling-parameter-dependent model for subthreshold swing S in double-gate SOI MOSFET's [J]. IEEE Electron Device Letters, 1994, 15 (11): 466–468.

[11] Colinge J P, Editors. FIN-FET and Other Multi-Gate Transistors [D]. Springer Journal of Multiphysics, 2008: pp 1-13.

[12] Amara A, Rozeau O, Editors. Planar Double-Gate Transistor: From Technology to Circuit [D]. Springe r Journal of Multiphysics, 2009: pp. 1-20.

[13] Moon Seok Kim, Huichu Liu, Xueqing Li, Suman Datta, and Vijaykrishnan Narayanan. A Steep-Slope Tunnel FET Based Sar Analog-To-Digital Converter [J]. IEEE Transactions on Electron Devices, 2014, 61(11): 3661-3667.

[14] Allen P E, Holberg D R. CMOS Analog Circuit Design. 2nd Ed [D]. New York: Oxford University Press, 2002.

[15] Vahid Baghi Rahin, Amir Baghi Rahin. A Low-Voltage and Low-Power Two-Stage Operational Amplifier Using FIN-FET Transistors [J]. Internatiuonal Journal of circuits and systems ,16, 3(4): 80-95.

[16] Agostinelli M, Alioto M, Esseni D, Selmi L. Leakage delay tradeoff in FIN-FET logic circuits: a comparative analysis with bulk technology [J]. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2010, 18(2): 232–245.

[17] Alioto M. Comparative evaluation of layout density in 3T, 4T, and MT FIN-FET standard cells [J]. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2011, 19(5): 751–762.

[18] Black W, Allstot D, Reed R. A high performance low power CMOS channel filter [J]. IEEE J. Solid-State Circuits, 1980, 6: 929–938.
[19] Dhulipalla L, Lourts D A. Design and implementation of 4-bit ALU using FIN-FETS for nano scale technology [C]. Nanoscience, Engineering and Technology (ICONSET), 2011 International Conference on, 2011; pp. 190-195.
[20] Duffy M., Dattoli E., Espinosa A. Nanoscale Silicon Technology. http://www.guo.ece.ufl.edu/project4.ppt.
[21] Jatkar M., Jha K.K., Patra S.K. First-principles investigation of F-functionalized ZGNR/AGNR for nanoscale interconnect applications [J]. J. Comput. Electron., 2021, 20: 1461–1470. https://doi.org/10.1007/s10825-021-01714-7
[22] Jatkar M , Jha K K and Patra. S K First Principle Investigations on Gas Molecules (CO_2, CO, NO_2, No and O_2) Using Armchair GaN Nanoribbons for Nano Sensor Applications [J]. IEEE Sensors Journal, 2022, 22(5): 3896-3902, doi: 10.1109/JSEN.2022.3144018.
[23] Gray P, Meyer R. Recent advances in monolithic operational amplifier design [J]. IEEE Transactions on Circuits and Systems, 1994, CAS-21(3): 317–327.
[24] Huijsing, J.,Hogervorst R, de Langen, K. J. Low-power low-voltage vlsi operational amplifier cells [J]. IEEE Transactions on Circuits and Systems, 1995, 42(11), 841–852.
[25] Islam A., Akram M, Hasan, M. Variability Immune FIN-FET-Based Full Adder Design in Subthreshold Region [C]. Devices and Communications (ICDeCom), IEEE International Conference, 2011: pp. 1-5.
[26] Johns, D., Martin, K. Analog Integrated Circuit Design [D]. New York: John Wiley & Sons, Inc., 1995.
[27] Suzuki, K., Tanaka, T., Tosaka, Y., Horie, H., Arimoto, Y., & Itoh T. Analytical surface potential expression for thin-film double-gate SOI MOSFETs [J]. Solid-State Electronics, 1994, 37(2): 327–332.
[28] Suzuki, K., & Sugii T. Analytical models for n+-p+ double-gate SOIMOSFET's [J]. IEEE Transactions on Electron Devices, 1995, 42(11): 1940–1948.
[29] Tosaka Y., Suzuki K., Horie, H Sugii, T. Scaling-parameter-dependent model for subthreshold swing S in double-gate SOI MOSFET's [J]. IEEE Electron Device Letters, 1994, 15(11): 466–468.
[30] Vinoth,C., Bhaaskaran, V. S. K., Brindha, B. & et al. A novel low power and high speed Wallace tree multiplier for RISC processor [C]. Proceedings of the 3rd International Conference on Electronics Computer Technology (ICECT '11), 2011: pp. 330–334.
[31] Wong H. S. P. Beyond the conventional MOSFET [C]. Proceeding of the 31st European Solid-State Device Research Conference, 2011: pp.69–72.
[32] Yu B., Wang H., Joshi, A., Xiang, Q., Ibok E., & Lin M. 15 nm gate length planar CMOS transistor [C]. Proceedings of the International Electron Devices Meeting. Technical Digest (IEDM '01), 2001: pp. 937–939.
[33] Vasudeva, G. Uma B V. 22nm FINFET Based High Gain Wide Band Differential Amplifier [J]. International Journal of Circuits, Systems and Signal Processing, 2021: 55-62.
[34] Vasudeva G, Uma B. V. Low Voltage Low Power and High Speed OPAMP Design Using High-K FinFET Device [J]. WSEAS Transactions on Circuits and Systems, 2021, 20: 80-87.