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Study on Multilevel Converter Main Circuit Topology Analysis and Modulation Simulation

Fei LV [a,1], Mian WANG [a] and Fenggang ZHAO [a]
[a] *Electromechanical Department, Naval Petty Officer Academy, Bengbu, China*

Abstract. With the development of power electronics, larger capacity is required. Multilevel inverter technology has been widely applied in high power equipment due to its advantages, including low voltage stress on power switches, low harmonics and EMI. However, when number of level increases, the multilevel topology and control method will be complicated, which will decrease the inverter's reliability. High capacity is the main development direction of power electronics technology in the future, multilevel converter technology is the key to realize high voltage high capacity, and the main circuit topology of multilevel conversion device is the focus of research. Multilevel converter technology becomes the key to realize high voltage and large capacity. With the increase of level number, the complexity of circuit topology and control increases, which reduces the reliability of the converter system.The article analyzes in detail several specific main circuit topology structures of multilevel conversion devices, points out the advantages and disadvantages of several topologies, analyzes and studies the reliability of cascaded multilevel conversion devices, and carries out Carrier Phase Shift Pulse Width Modulation(CPSPWM)Simulation analysis.

Keywords. Multilevel converter, main circuit topology, switch status, multi-carrier modulation

1. Introduction

The birth and development of power electronics technology has revolutionized the way humans use electrical energy. The development of power electronics requires power electronics devices to output electrical energy with increasing capacity, quality and reliability [1]. Large capacity is the main development direction of power electronics technology in the future, the way to achieve high capacity are high voltage, high current, in practice high voltage high capacity is commonly used, and multi-level conversion technology is the key to achieve high voltage high capacity. From the introduction of the concept of multilevel conversion device to date, it has formed a variety of basic topologies and a series of improved topologies [2-6].

In this paper, several specific topologies of multilevel converter are analyzed in details, the advantages and disadvantages of several topologies are pointed out, the reliability of the cascaded multilevel converter is studied, and the multi-carrier

[1] Fei LV, Corresponding author, Electromechanical Department, Naval Petty Officer Academy, Bengbu, China; E-mail: lf19828050@163.com.

modulation simulation analysis of the three-phase cascaded 11-level converter is carried out.

2. Multilevel Converter Main Circuit Topology Structure

2.1. Diode-clamped Multilevel Topology

A single-arm circuit topology of a diode-clamped three-level converter is shown in figure 1(a). Four switching devices S1-S4 are connected in series for each phase of the bridge arm, and each two switching devices are on or off at the same time, where (Sl, S3) and (S2, S4) are complementary operating switching pairs; Dl, D2 are clamping diodes.

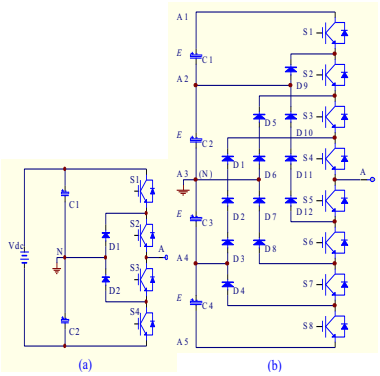


Figure 1. DCMI Topology.

Table 1. Single-phase 5-level DCMI output voltage versus switch status.

Output voltage	Switch status							
	S1	S2	S3	S4	S5	S6	S7	S8
2E	1	1	1	1	0	0	0	0
E	0	1	1	1	1	0	0	0
0	0	0	1	1	1	1	0	0

The same principle is used to extend the converter to more levels. Figure 1 shows the topology of a single-phase bridge-arm five-level DCMI. The output voltage of DCMI and its corresponding switch status are listed in table 1. When the number of levels is odd, the neutral point N is physically present, while when the number of levels is even, the neutral point N is virtual and cannot be directly induced.

2.2. Flying-capacitor Based Multilevel Topology

The Flying Capacitor Multilevel Inverter (FCMI) topology was first proposed by H. Foch at the PESC conference [7]. A typical topology of single-phase FCMI is shown in figure 2(a). S1-S8 in figure 2(b) are power switching tubes, C5-C10 are clamping

capacitors, each with the same capacitance value and voltage, and Cl-C4 are DC voltage divider capacitors. FCMI uses fly-across capacitors instead of clamping diodes to achieve the voltage clamping function. From the FCMI switch status and the corresponding output voltage relationship, it can be obtained that the FCMI voltage synthesis is more flexible, for the same output voltage, can be obtained by different switch status combinations. For example, output voltage E, corresponding to four switch status combinations; output voltage 0, corresponding to six switch status combinations. This redundancy of switch status combinations provides the possibility and flexibility for fly-across capacitor voltage balancing and, at the same time, provides a possible line for reconfiguration of fly-across capacitor type multilevel conversion devices.

Compared to the diode-clamped type, the fly-across capacitor type removes a large number of clamping diodes, but introduces a large number of suspension capacitors with lower reliability and shorter lifetime.

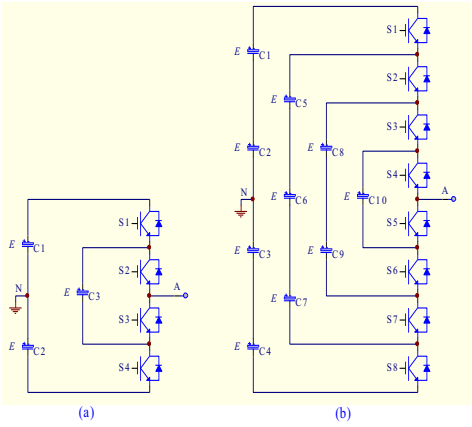


Figure 2. Main circuit topology structure of single-phase fly-across-capacitor multilevel (FCMI).

2.3. Generalized Multilevel Topology

F.Z. Peng proposed a generalized multilevel converter topology, which makes the study of multilevel converter topology more systematic [8].

Figure 3 shows the single-phase generalized multilevel converter topology. In this circuit, the switching devices Sp1-Sp4 and Sn1-Sn4 are the main switching tubes, which are used to achieve the desired output level, and Sc1-Sc12 are the clamping switches, which are used to achieve the clamping function. The two complementary switches (e.g., Sp1 and Sn1), when one is on, the other is off. The voltage synthesis of general-purpose multilevel topology is more flexible, for the same output voltage, can be obtained by different switch status combinations, such as 0 voltage output corresponds to 6 switch status, that is, there is redundancy in switch status combinations.

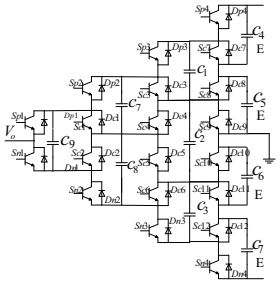


Figure 3. Single-phase general purpose 5-level main circuit topology structure.

2.4. Cascaded Multilevel Topology

Figure 4(a) shows the conventional single-phase cascaded five-level topology, consisting of two H-bridges cascaded [9-11].

The cascaded type does not require a large number of clamping diodes and fly-span capacitors compared to the diode-clamped type and fly-span capacitor type, and by using different DC voltages for different H-bridge units, more output levels can be obtained than using the same DC voltage. As shown in figure 4(b), the same number of H-bridge units with 1:2 DC voltage can obtain 7 output levels.

Advantages of cascaded multi-level: (1) Adopting mutually independent DC power supply, no need for static and dynamic voltage equalization. (2) With modular structure, internal redundancy can be reconfigured. (3) For the same number of levels, the cascaded structure requires the least number of components.

Disadvantage: Multiple independent DC power supplies are required.

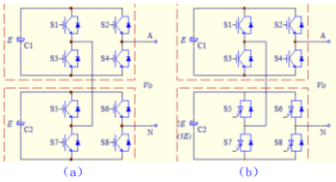


Figure 4. H-bridge cascaded multilevel converter main circuit topology structure.

2.5. Hybrid Multilevel Topology

The hybrid clamped multilevel shown in figure 5(a) is a multilevel topology that uses diodes and capacitors together for clamping. The starting point of this topology is to solve the problem of unbalanced capacitor voltage at the dc terminal and blocking of higher voltage by the internal switching device in the conventional diode-clamped multilevel topology. The fly-across capacitor in this topology is involved in voltage synthesis. Due to the presence of clamping diodes, this topology has more current paths. This topology uses the redundant switch status of the intermediate output levels to achieve capacitor voltage balancing, but not in the case of pure reactive power.

In figure 5(b), Sal-Sa4 and Snl-Sn4 are the main switching tubes used to achieve the desired output voltage; Scl-Sc6 are clamping switching devices, Dcl-Dc12 are clamping diodes, and C5-C7 are auxiliary capacitors, which together achieve the

clamping function; the voltage balance of each capacitor C1-C4 on the DC side is guaranteed.

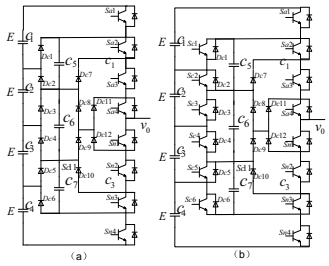


Figure 5. Multilevel topology with hybrid clamping.

3. Three-phase Cascaded Multilevel Topology

3.1. Three-phase Cascaded Multilevel Reliability

The main circuit of the three-phase cascaded multilevel converter is shown in figure 6.

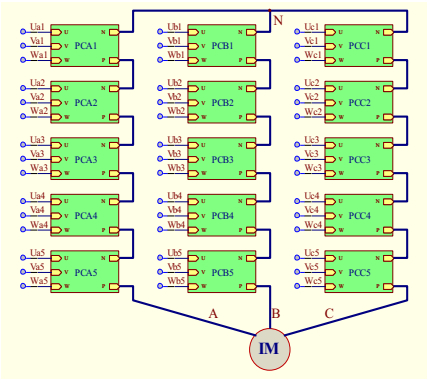


Figure 6. Main circuit of three-phase cascaded multilevel converter speed control system.

Figure 6 shows the main circuit of a three-phase cascaded multilevel converter speed control system, where PCA1,..., PCA5, PCB1,..., PCB5, PCC1,..., PCC5 are all cascaded power conversion units.

The reliability of a multilevel inverter speed control system is determined by both the reliability of the unit and the reliability of the system (fault reconstruction capability). Even if the reliability of the unit is high, if the fault reconstruction capability of the system is poor, the overall reliability of the system can hardly be guaranteed. If the system has no reconfiguration capability, the reliability of the system is r^m, and if the system has the reconfiguration capability to allow a module failure, the reliability of the system is $r^m + mr^{m-1}(1-r)$ [12].

The system shown in figure 6 consists of 15 units, and if reliability is expressed as a percentage, when the system is not fault tolerant, the reliability of the system is only 86% even if the individual reliability is 99%. When the system can tolerate a unit

failure, the reliability of the system can reach 99%, which is 13% higher than when the system is not fault tolerant.

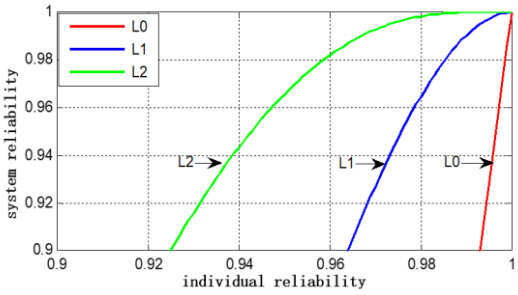
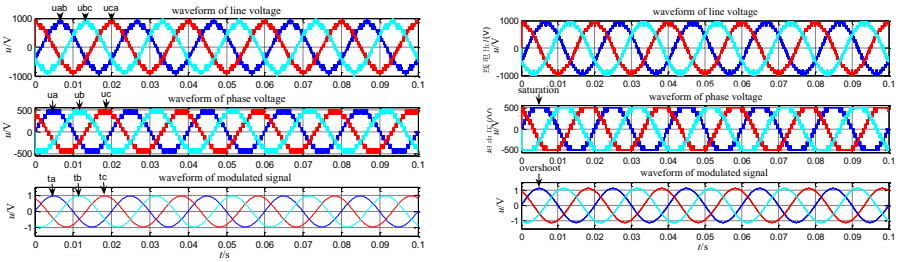


Figure 7. Relationship between system reliability and individual reliability (15-unit).

Figure 7 shows the correspondence between system reliability and individual reliability when the 15-unit system has the reconfiguration capability of 0, 1, and 2 unit module failures, respectively. The relationship between the curves in figure 7 shows that the higher the reconfiguration capability of the system, the higher the reliability of the system when the individual reliability is the same.

3.2. Simulation of Three-phase Cascaded Multi-level Multi-carrier Modulation

Carrier phase shift pulse width modulation (CPSPWM) is generally used in the cascaded multilevel converter whose basic principle: each cell module of the multilevel converter uses a single-phase SPWM with low switching frequency, and each cell module has the same amplitude modulation ratio (M_a), and frequency modulation ratio (M_f), but there is a certain phase difference between the carriers of each cell module, and the total output of the converter is a linear superposition of the output of each cell module. CPSPWM can reduce the output harmonics without increasing the switching frequency.



(a) (M_f=10, M_a =0.95, m=5) (b) (M_f=10, M_a =1.1, m=5)

Figure 8. Simulated output waveform of three-phase cascaded 11-level converter CPSPWM.

Using MATLAB for simulation, figure 8 shows the waveforms of phase voltage, line voltage and modulating signal of the CPSPWM simulation output of the three-phase cascaded 11-level converter. Among them, figure 8(a) simulation parameters: M_a=0.95, M_f=10, figure 8(b) simulation parameters: M_a=1.1, M_f=10; frequency is 50Hz.

From the simulation waveform shown in figure 8, the analysis shows that: (i) The Carrier Phase Shift Pulse Width Modulation (CPSPWM) method can realize the control of a Multi-level cascaded converter; (ii) The maximum amplitude modulation ratio of the CPSPWM method is one, and the output voltage saturates when $M_a$is greater than one.

4. Conclusion

Multilevel conversion technology is the key to achieve high capacity and high voltage, and the main circuit topology of multilevel conversion device is the focus of research. In this paper, we analyze several specific main circuit topology structures of multilevel converter, point out the advantages and disadvantages of each type of topology, study the reliability of three-phase cascaded multilevel converter with cascaded multilevel as the object, and verify the multi-carrier modulation simulation analysis of three-phase cascaded 11-level converter. Multi-level topology optimization improvement and application will be the next research focus.

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