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Analysis of Different Configurations of $Si_{1-x}Ge_x$ for Double-Gate MOSFETs and Its Future Applications

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Abstract. The major drawbacks of basic electronic components i.e., Vacuum Tubes used before the 1960s were a large size and the inability of these to be scaled down further. With the emphasis shifting to scaling down we came across the MOSFETs in single-gate configuration since the 1960s, they are utilized nowadays in the nanometer region for keeping the high-performance level but still, these single-gate configurations of MOSFETs suffer from different parameters such as coupling, interfacing, channel mobility, channel orientation, switching delay, latch-up and leakage current, short channel effects (DIBL, GIDL, subthreshold swing) and volume inversion and this has led to decrease in inversion charge, increase in leakage current and reduction in the drive current leads us to the exploration of the double-gate configuration of MOSFET and on further exploration it leads us to the novel and higher mobility channel materials such as $Si_{1-x}Ge_x$ which can perform and even shows better results than prevailing single-gate MOSFETs. This paper analyses the different configurations of $Si_{1-x}Ge_x$ for double-gate configuration of MOSFETs and its Future Applications.

Keywords. Double-Gate MOSFET, $Si_{1-x}Ge_x$, Scaling Parameters, Subthreshold Swing, Threshold Voltage.

1. Introduction

Since the early 1930s research has been carried out to find the configuration that likely replaces Vacuum Tubes. As a result, in 1960 single-gate MOSFETs, and 1965 Moore's Law came into existence [1]. The MOSFET shown in Figure 1 is a three-terminal voltage-controlled device working like a switch, either fully on at input drive or fully off at zero current by keeping the multiple of supply voltage or itself [2]. Moore's Law shown in Figure 2 elaborates that for a particular area, the number of transistors doubles for nearly 18 months, this leads to acclimation of the multiple numbers of transistors in the defined area by continuously decreasing dimensions (scaling) [3-7]. It is done to accommodate performance with minimum power consumption and power dissipation.

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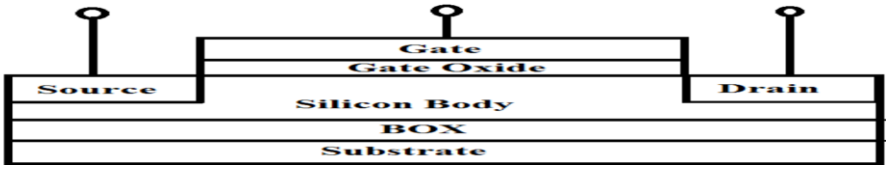

Figure 1. Structure of Single-Gate MOSFET.

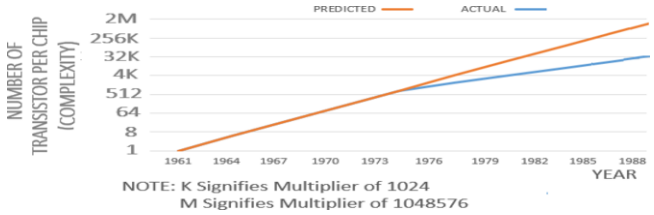

Figure 2. Interpretation of Moore's Law.

While doing so, we came across some limitations in form of Short Channel Effects (SCE), summarized in Table 1 [8-11]. To overcome them, new configuration double-gate MOSFETs shown in Figure 3 came into existence. Here, two gates are available on opposite sides, separated by the gate oxide operating simultaneously. This gives better current in the drain and ensures gate control over the channel and gate coupling [12-14].

The main motivation and purpose behind this research work is

- To provide the solution to problems associated with scaling.
- To minimize the limitations of single-gate MOSFETs.

This has guided us to define our problem statement as

- How to conserve drive current?
- How to depreciate the leakage current?

Thus, for the problem statement defined above our research focuses on

- Understanding the device physics.
- Analyzing the behavior of the device through simulation.

The main objectives of our proposed research work are

- To review the conventional work done in the field of double-gate MOSFET configurations simulated so far.
- To analyze the device physics of different configurations of $Si_{1-x}Ge_x$ double gate n-MOSFET and the behavior of the device through simulation.
- To examine the I_d-V_g characteristics, I_d-V_d characteristics, and performance parameters DIBL, MMCR, Subthreshold Slope, and Threshold Voltage.

Table 1. Major Short Channel Effects

Short Channel Effects	Reason Of Existence
DIBL	Drain Induced Barrier Lowering. This comes into effect when we increase drain voltage to the point that there is a decrease in the potential barrier of the channel. This leads to the movement of electrons between the source and drain without any resistance which too when the gate voltage is lower than the threshold voltage.

Subthreshold Leakage Current	This comes into the effect when came into effect when a weak inversion conduction region is generated in the presence of a hot-electron effect because of which when the gate voltage is less in comparison to the threshold voltage, diffusion current flow takes place between drain and source.

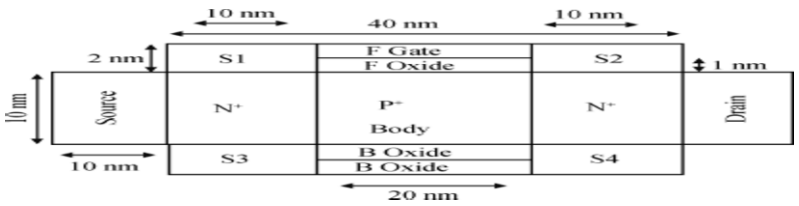

Figure 3. Structure of Double-Gate MOSFET.

2. Literature Review

The different configurations of $Si_{1-x}Ge_x$ utilized by researchers so far provide a balance between electron mobility and hole mobility of Ge are summarized in Table 2.

Table 2. $Si_{1-x}Ge_x$ configurations, Gate configurations, and their applications

$Si_{1-x}Ge_x$ and Gate Configuration	Reference	Applications
$Si_{0.2}Ge_{0.8}$	[15-16]	Thermoelectric Applications
Schottky Barrier	[17]	Leakage Current Improving Applications
SiGe Shell	[18]	Ultrathin P-FinFET Applications
Sub 100 nm Tunnel FET	[19]	DRAM Applications
Heterojunction Tunnel Model	[20]	Optimize Tunnel Logic Inverter Applications
Negative Capacitance	[21]	Tradeoffs in Energy Delay Low Power Switching Applications
Heterogeneous Tunnel Dielectric	[22]	Device Reliability Applications
Gate Surrounding Channel	[23]	6-Transistor SRAM Cell Applications
Vertical Slit	[24]	3-DM Integration Applications
Fully Depleted SOI	[25]	Radio Frequency Applications
SiGe	[26]	Enhancing Speed and High-Volume Optical Interconnect Applications
$Si_{0.6}Ge_{0.4}$	[27]	Step-FinFET and Inverter Applications
Gate All-Around	[28]	SCE Improvement Applications
Double-Gate	[29]	High Pass Filter Applications
Double-Gate	[30]	Core Insulator Applications
Double-Gate	[31]	Fully Depleted SOI Applications
Dual-Gate	[32]	Source Follower Applications
Memristor	[33]	Reducing Power Consumption and Increasing IC Performance Applications.

3. Results and Discussion

We have studied, compared, and analyzed the different configurations and summarized the results in Table 3, Table 4, Table 5, Figure 4, and Figure 5 for $Si_{1-x}Ge_x$ configurations. Additionally, we have compared results with pre-existed configurations from papers [15 and 16] and it possesses some advantages as well as some disadvantages listed below. The results obtained show that for $Si_{1-x}Ge_x$ double-gate MOSFET performs better in comparison to single MOSFET. Its advantages are

- Dissipates less power.
- Dynamic control of voltage.
- Gate electrostatic control in conducting channel is better.
- Large degree of reliability.

Its disadvantages are

- Subthreshold Swing is higher.
- Leakage Current is higher in the subthreshold region.

Table 3. Different Configurations of $Si_{1-x}Ge_x$ used

Configurations of $Si_{1-x}Ge_x$	Single Gate	Double Gate
Si	Utilized	Utilized
$Si_{0.2}Ge_{0.8}$	Utilized	Utilized
$Si_{0.6}Ge_{0.4}$	Utilized	Utilized

Table 4. Single-Gate MOSFET using $Si_{1-x}Ge_x$ and Double-Gate MOSFET using $Si_{1-x}Ge_x$

Performance Parameters	Single Gate MOSFET using $Si_{1-x}Ge_x$ [16]	Double Gate MOSFET using $Si_{1-x}Ge_x$
Bandgap of Channel Material	Multiple of 1.12 eV	Multiple of 0.66 eV
Drive Current Delay	In the Range of 0.1 ns	In the Range of 0.05 ns
Electric Field	$3*10^5$ Vcm^{-1}	10^5 Vcm^{-1}
Electron Mobility of Channel	Magnitude Order of 1500 $cm^2V^{-1}s^{-1}$	Magnitude Order of 3420 $cm^2V^{-1}s^{-1}$
Hole Mobility of Channel	Magnitude Order of 450 $cm^2V^{-1}s^{-1}$	Magnitude Order of 1610 $cm^2V^{-1}s^{-1}$
Off-State Leakage Current	More than 1 $nA\mu m^{-1}$	Less than 1 $nA\mu m^{-1}$
Power Dissipated	In Between 0.5 Js^{-1} and 0.7 Js^{-1}	In Between 0.1 $Js^{-1}$and 0.3 Js^{-1}
Threshold Voltage	In Between 350 mV and 450 mV	In Between 100 mV and 300 mV

Table 5. Double-Gate Configuration for pure Si and for $Si_{1-x}Ge_x$ (x = 0.8 i.e., $Si_{0.2}Ge_{0.8}$)

Performance Parameters	Double-Gate using pure Si [15]	Double-Gate using $Si_{1-x}Ge_x$ (x = 0.8 i.e., $Si_{0.2}Ge_{0.8}$)
DIBL	80 mdB	66.66 mdB
MMCR	$1.3*10^8$	$2.7*10^8$
Subthreshold Swing	82.23 mV/dB	86.84 mV/dB
Threshold Voltage	In Between 100 mV and 300 mV	In Between 100 mV and 300 mV

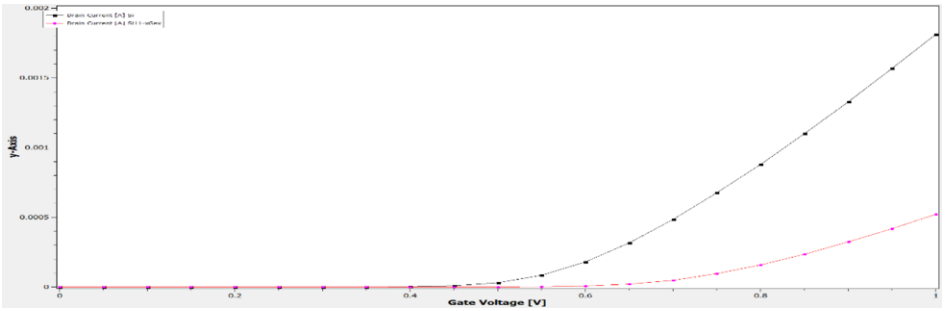

Figure 4. Comparing I_d-V_g characteristics of double-gate configuration for pure Si and double-gate configuration for $Si_{1-x}Ge_x$.

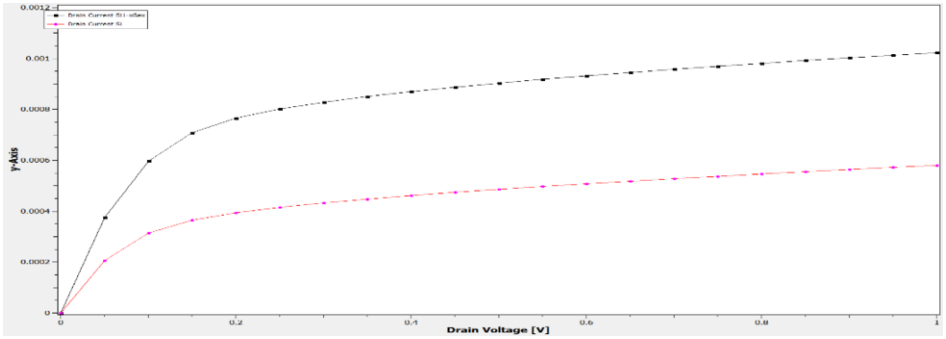

Figure 5. Comparing I_d-V_d characteristics of double-gate configuration for pure Si and double-gate configuration for $Si_{1-x}Ge_x$.

4. Conclusion

We measured certain performance parameters in the previous section and measured values are defined already in Table 5. From this analysis, one can conclude that $Si_{1-x}Ge_x$

- Has a very encouraging future in form of capabilities i.e., high carrier mobility, high speed, low power consumption, and low power dissipation.
- Can replace Si in the coming decade once performance parameters are taken into consideration.
- Meets all the provisions for sustaining the ICs design in the CMOS circuit designing, especially in the electronics and communication industry.

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