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# High Performance Area Efficient Scalable In-Place Real Valued FFT

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**Abstract**. An approach for formulating an area-latency and optimized architecture for an in RFFT is outlined in this study. In this paper, modified butterfly block with an addition of re programmable clock divider for generation of variable clock has been proposed. Because of its numerous uses in traditional digital signal processing and other developing domains, efficient computing of the real-valued Fast Fourier transform (RFFT) has got attention in recent years. Scalable in-place RFFT structure for larger inputs and efficiency with high throughput which is an important scenario that leads to the increase in size of memory and accessing issues of storage memory. A butterfly block, that does the computations of butterfly unit per clock period, is typical in an in-place FFT configuration. Study suggests that the in-place FFT can significantly improve the butterfly block structures and thereby providing reduction in parameters such as area occupancy and time delay. However, by changing the structure of butterfly blocks at higher input implementations, fourier transform calculations can be made such that good efficiency is obtained. Every application has several modules that run at different speeds, that needs clock which can be programmable according to the application's parameters. To address this, a reprogrammable clock divider was implemented, and the parameters efficiency was studied and determined to be improved timing and area to existing implementations. The proposed method is implemented using Xilinx ISE 14.7 and the area, delay of existing and implemented designs are compared.

**Keywords.** Fast Fourier Transform (FFT), Butterfly block, RFFT, twiddle factors, storage unit.

## I. Introduction

Discrete FT is a technique that converts specific sorts of function sequences into function of frequency representations. A fast Fourier transform (FFT) is a mathematical computational model that is used to perform the discrete FT of a sequence. DFT demands for N2 floating-point multiplications for evaluation and calculation. As the constraint integer values of i and k always change, many of the multiplications should be performed repeatedly. The FFT is a systematic way of approach which is aimed and focused at reducing the number of redundant which means unnecessary repeated calculations. In VLSI architectures, pipeline topology of FFT can be segregated as single-path delay feedback (SDF) and MDC based structures. Apart from pipeline, one more variant of

FFT that is based on the memory of processor is a folded base in-place formations. Most of these structures have 3 parts: (i) the operation in butterfly, (ii) the memory storage part, and (iii) the twiddle value generation circuit. Internal and intra based butterfly portion calculations that are reciprocated or folded symmetrically in the BCU for low-complexity realization in PM-based structures, is considered as merits for in-place based FFT and benefit to the application.
Signal processing devices can analyze and handle data input or output information sequences for both special and spectral domain. FFT widely applied on real-valued data in scenarios that are including voice, audio, graphic, and video processing. With rise in medical field of processing the signals in systems & the multiple uses of real numbered spacial data analysis, efficient realization of FFT on real signals got a lot of attention presently. Conjugate symmetry emerges in the FFT of a real numbered signal, that makes 50 percent of the FFT outcomes to be unnecessary that can be removed. The discrete FT, which relates length-N series data shots to its length-N complex spectral elements that can be easily computed numerically that by using the FFT mechanism. Although all Fast FT methods can be developed and implemented for calculating Discrete FT of complex number, real-valued sequences are frequently modified. The Discrete FT of length-N real-number segment can also be computed using length-(N / 2) complex FFT algorithm and is recognized that by utilising symmetries within complex-valued algorithms, more efficient algorithms can be constructed.

In DIF FFT algorithms, the output spectral domain sequence X(k) is arranged into even index value as well as odd numbered index value and uses a natural order input sequence. In addition, DFT should be read backwards in time. In DIT FFT algorithms, the input data sequence is split into even and odd numeric instances called bit reversal order and the output sequence is natural.

## 2. Earlier Work

Let the numbers x0,x1,x2,...xn be complex. The formula for the N-point DFT is:

$$X_k = \sum_{n=0}^{N-1} x_n e^{-j\frac{2\pi k}{N}n} \quad , k = 0, 1, \ldots, N - 1 \ (1)$$

A byte of data in addition to values of TF derived using mathematical expression involving cosine and sine values obtained from twiddle factor value holder unit and is transferred to computation block which arithmetic step for every clock cycle.

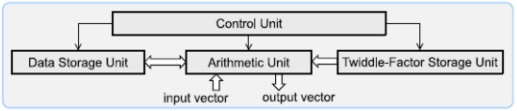


**Figure 1.** Existing structure for in-place RFFT

The circuit for DIT RFFT in-place processing [11] is available in figure 1. The ALU units consists of butterfly operations that is performed in FFT whereas the data storage and

twiddle factor storage unit are to store the internal data and twiddle factor multipliers data respectively. To monitor this operation, a control unit is required. The block diagram of control unit [14] consists of counter and multiplexers, counter and AC indicates the AND cell.

Atleast 1 data information is required and collected from the very same bank per 1 clock period, accessibility problems occur. The entry retrieving problem can be addressed & resolved by shifting the location of the samples in a particular row by shifting operation, that is performed on the information samples of each data block in combinations of two data samples, it can be before or after they can be stored & read in/from the register banks at the same time respectively. The storage unit [14] uses two data-swapping circuits to resolve bank conflicts and reorder input-block samples (DS1 and DS2).

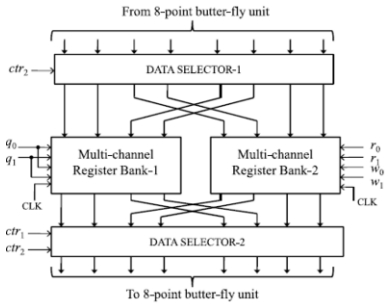


**Figure 2.** SU block

Based on earlier works [9], the construction of memory device is based on design table having points of thirty two in number along with a four in size of butterfly tasks performing circuit design[12]. Figure 2 illustrates an optimised block [14] for storing the variable data consisting of twiddle factors that is designed for a thirty two point real number Fourier FT that includes eight point sized butterfly computation architecture. It uses a single 5 4w ROM LUT, as w defines the size or width consisting of the real number constraint related to twiddle factor constants cl, sl. Twiddle factor unit [14] has the control bits s1, s0 which are the selection lines of inputs to the block multiplexer that is used for choosing bottom address values with bit size two in number, each of the butterfly evaluation task performers which are five in number in a real numbered fast FT with a points of thirty two formed using {q4, q3, q2}.

Data Selectors [14] DS-1 and DS-2's interior structures consists of multiplexers with control signals ctr 1 and ctr 2. Each DS receive/send a pair of data samples from/to the BCU. The signal ctr2 controls the shifting of data between the two information selector blocks. During DS-1 swapping procedure, the signal ctr1 is set to '1.' MUX1 to MUX4, and MUX5, MUX6 exchange data to cancel DS-1's switching action

## 3. Proposed Work

SU design

In the proposed work, 8 point butterfly unit is changed as two 4-point butterfly units as in figure 3 to implement 32 point FFT as in figure 3. With such butterfly structure, number

of twiddle factors and design complexity can be reduced. A design methodology for developing area efficient with a reduced delay is used to implement in place calculation of real valued fast FT. MCRB [14] depicts the implementation design of the Multichannel Reg. Bank. It has 16 registers, four rows and four columns. R11, R12, R13, R14 form Bank-1, while R41, R42, R43, R44 form Bank-4.

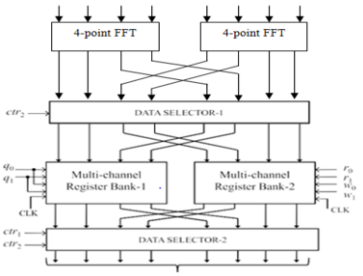


**Figure 3.** Proposed FFT structure for butter fly unit and storage device

Programmable clock divider

To address requirements of variable range and rate of performance constraints in phase detection methods, a dynamic line selection based fully reconfigurable frequency divider is proposed. The rate-controller asserts delay line consists of inverters and a gate chain that is driven by the input sample rate. In order to achieve the clock skew design standard, each logic cell chain is connected based on unit delay. PLL is used for synchronous clock generation system to drive counter at variable rate. This technique enables for the deployment of a single input source clock through many different rate clock domains. A fully programmable or re configurable clock divider might divide a input source clock into any integer multiple of clock periods. Using proper clock down sampling and synchronising events, the ideal operating speed of the buffer state transition is determined. The suggested architecture uses reconfigurable delay lines and is directly generated as buffers, whereas the typical PLL VCO for phase synchronisation is complex in nature.

A decoder circuit with two input design enabling clock enabling a few register rows related to different banks of four in number, utilized to write the incoming data x1, x2, x3, x4 related to a single block with decode output as an address of the content for writing (w0,w1). The content of each bank's four registers is accessible via the multiplexer, based on r0, r1. At every clock signal, 4 outputs are retrieved at 4 banks of each multichannel, as 1 frame of a byte of data gathered from MCRB-1 and MCRB-2 to successfully complete butterfly operations of stage number i, while intermediate outputs can be returned to previously assigned locations over successive clock period level/ edge for every next level butterfly mathematical calculations.

## 4. Experimental Results

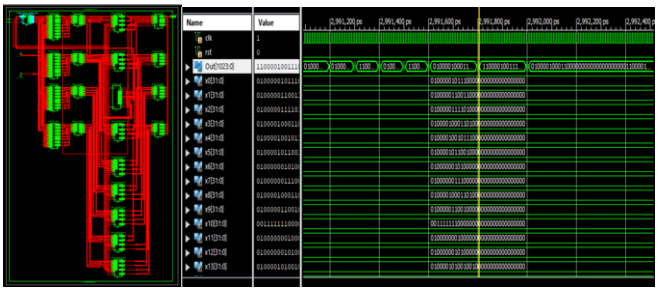

**Figure 4.** RTL schematic & Simulation results for FFT

Figure 4 shows RTL schematic and simulation results for implemented design. Clock signal with positive edge triggering and high reset signal for first clock cycle, the output is zero irrespective of other computations. For next clock cycle, with reset low, FFT inputs along with generated control signals and twiddle factor values, generates final output FFT process for every 10 clock cycles, due to modulus 10 programmable counter and there is variation in the delay for different clock rates.

| Parameter | Existing FFT | Proposed FFT |
|---|---|---|
| Delay(ns) | 39.458 | 17.427 |
| Area(LUT's) | 10746 | 4084 |

**Table 1.** Comparison between Existing and Proposed methods.

Table 1 describes the comparison in Area and Delay between FFT algorithm implemented with Existing and butterfly unit (Proposed) along with a reconfigurable clock rate. It is observed that there is reduction in area and delay with proposed FFT algorithm.

## 5. Conclusion

This paper presents a design development strategy for implementing an efficient and reliable Fast FT for in place calculations that is scalable with better throughput and can be designed for different sizes of FFT topologies. .In proposed design, 8 point FFT butterfly structure is implemented by using two 4 point FFT along with a programmable counter. Proposed implementation optimizes area along with optimized delay when compare to existing design. The synthesis and simulation results have been verified using Xilinx ISE 14.7 tool.

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