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Parallel Connection of Switches and Capacitors to a Voltage Source in a Multilevel Inverter

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Abstract. In this manuscript, a new seven-level (7-L) inverter circuit by means of a solitary dc basis, capacitors and switching devices is promoted. This topology employs only a single independent dc source, three dc capacitors, two diodes and seven switching devices. All the elements in the system are effectively utilized to generate the required the voltage level of output. This topological approach has higher reliability and lowers the harmonic distortion due to the fewer the system contains a lot of components and due to the production of a higher sum of stages in the output. The dc capacitors have the advantage of natural voltage balancing due to symmetric production voltage stages in this topology. The operating modes and Detailed description of the modulation method of the suggested structure. In the SIMULINK/ MATLAB environment, the proposed network topology is also simulated with the results.

Key words: Multilevel configuration; Single DC source; Reliability; Consonant alteration.

1. Introduction

A multilayer inverter was widely adopted by the first multi-level, high-voltage, high-power industry that benefited from its use. At the output, sinusoidal waveforms are also expected to be generated. We can ensure a low THD output with a wide range of voltages, a small output filter size, and little dv/dt stress. However, numerous circuit components are necessary [1-4]. A "cascaded H-bridge (CHB)" inverter is one of the best techniques to increase the number of output voltage levels in a modular, straightforward manner [5-7]. Increasing CHB has the drawback of necessitating more DC tension sources, H-bridge cells, and switches. Utilizing asymmetrical dc voltage sources is one technique to minimize the number of parts in a CHB [3]. When the DC tension is three, the output voltage is at its highest. Nevertheless, initiatives are being taken to increase the output voltage of various DC power sources. A multilevel converter with a cascaded transformer has been installed to solve this problem. It also uses an asymmetrical voltage source combination to synthesize the output voltages at multilevel. The best thing is that it only uses a single source of dc voltage [8-12]. However, since the system works in low frequency a cascaded transformer is voluminous. The multi-level inverter was introduced in to mitigate this problem using four fluid power supplies. But to get independent dc

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voltage sources, a front-end transformer is needed. Transformer less circuit topologies were implemented in order to overcome this problem. In general, CHB updated and built these kind of multi-level inverters. A multilevel inverter packed U cells was given [13-17]. It demonstrates excellent output in circuit components reduction.

However, drive losses increase when each voltage level is generated by three switching devices for each level generation, because the current is circulating at each level [18-20]. In addition, voltage over the condenser has fantastic waves even though it uses a bulky 5000 μF condenser. In (E. Babaei, et al., 2008) were proposed multi-level inverters using bidirectional and Series-related switches [7, 21, 22]. In principle, with the limited number of circuit components they can produce more than 125 output voltage levels. In order to obtain dc voltage source, each condenser requires a dc-to-dc converter [8]. In a modular converter of multilevel has been implemented. It has a modular construction, making it easy to add more voltage. However, more bulky condensers and switches are available than previous choices. It was suggested that multi-level inverters use series-related DC voltage sources [9, 19]. It consists of a step to generate the level and an architecture to minimize the losses of switching. However, no components can be designed to reduce the amount of power source dc if the voltage level is increased. The multilayer inverter serial/parallel dc voltage was introduced around the time of -> The multi-level inverter was introduced with series/parallel dc voltage sources around the time of switching [10, 16, 23]. Conduction losses are also enhanced and switching patterns are convoluted. The boosting type inverters are forming a new trend in the family of "DC-AC converters". In this group, "Current Feedback Static Inverter (CFSI)" are the traditional and outmoded types [11]. T-type converters are forming a major part of the family of multilevel inverters (MLIs) [14]. A basic single-phase T-type converter can produce three-level A.C output across the load terminals [12, 13, 14, 15, 17, 18].

2. System Description

Figure 1 is a depiction of the recommended converter. The 7-L AC output voltage is produced using a single-phase PWM inverter. The converter uses seven bidirectional interrupters, two unidirectional diodes, one dc tension, and three dc condensers. Despite the two-way conductivity of the switching devices, the anti-parallel diodes only allow the tension to pass in one direction. The condensers in the dc bus are connected in series to a dc voltage source. The DC supply, which can be accessed via a battery bank, PV systems, or rectifier circuits, can be utilized in the recommended topology. The dc capacitors are termed as C_1, C_2 and C_3. The dc capacitors are charged to a voltage of $V_{dc}/3$ each, in the steady-state.

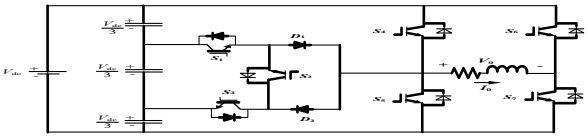
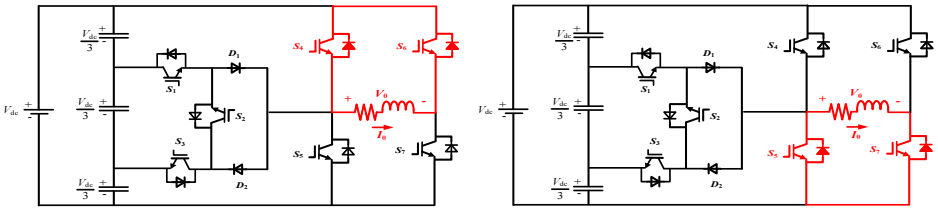
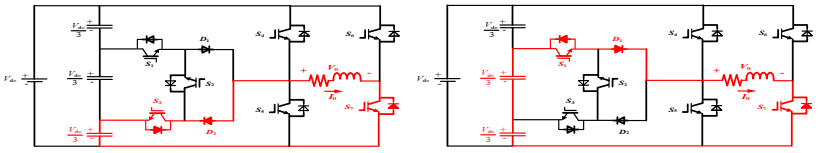


Figure 1. Schematic Diagram of the Proposed Inverter

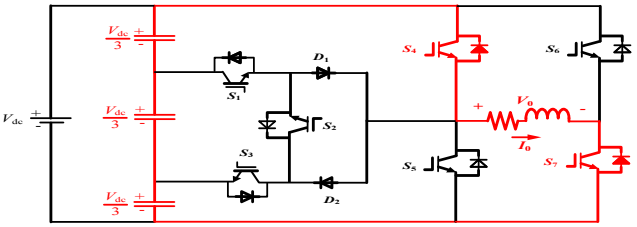


(a) (b)

Figure 2. Functioning modes during nil crossing: (a) $V_0 = 0^+$ and (b) $V_0 = 0^-$

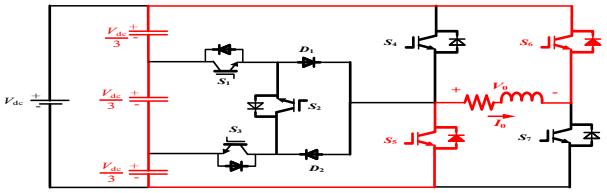


(a) (b)



(c)

Figure 3 Positive level operating modes: (a) $V_0 = V_{dc}/4$, (b) $V_0 = 2V_{dc}/2$ and (c) $V_0 = V_{dc}$



(c)

Figure 4. Modes of Operation at Negative Voltage $V_0 = -V_{dc}$

3. Modulation Techniques

Table 1 provides an overview of the status of the switches in the proposed converter, which makes it easier to describe their operation. Table 1 shows that IGBTs 1 and 0 are in the "on" and "off" positions, respectively, as shown in Figure 1. As a result of their lower frequency, the S5 and S6 switches lose less when switching. In the suggested architecture for IGBT gate pulse creation, Figure 5 depicts the modulation technique used. A pure sinusoidal waveform is superimposed on six triangular waveforms. The sinusoidal wave is the transporter wave, while the sinusoidal wave is the reference wave. Carrier waves 1, 2, 3, 1', 2', and 3' are in contact with the reference wave at defined intervals. As a result, the signal emitted consists of P1-P3 and N1-N3 pulse patterns. The appropriate output voltage is produced using logic entrance circuits, and effective

utilization of the pulses has been applied to the process. To manage the level of output, the "Modulation Index (M.I.)" is configured like this:

$$M.I. = \frac{V_{0peak}}{3 \times V_{dc}} \tag{1}$$

Table 1. Substituting positions of the projected system

Output Voltage level (V_O)	S1	S2	S3	S4	S5	S6	S7	D1	D2
V_{dc}	0	1	1	1	0	1	1	0	0
$2V_{dc}/3$	1	0	0	0	0	1	1	1	0
$V_{dc}/3$	0	0	1	0	0	0	1	0	1
0^+	0	0	0	1	0	1	0	0	0
0^-	0	0	0	0	1	0	1	0	0
$-V_{dc}/3$	1	0	0	1	1	1	0	1	0
$2V_{dc}/3$	1	0	1	0	1	1	0	0	1
$-V_{dc}$	0	0	0	0	1	1	0	0	0

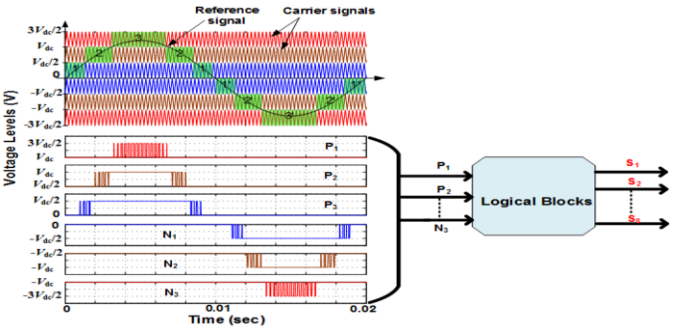


Figure 5. PWM system with sine-triangle analysis

Table 2. Regulatory Settings

Parameter	Value
Fundamental frequency (f_m)	50 Hz
Switching frequency (f_{sw})	4 kHz
I_0 (A)	3.5
V_0 (V)	230
P_{output} (W)	730
V_{dc} (V)	240 V

4. Simulation Results

To demonstrate the usefulness of the suggested configuration, we run a "MATLAB" simulation. For our simulation, we'll utilize a single-phase output voltage of 230 V and a frequency of 50 Hz. The remaining simulation work parameters' values are in Table 2. Voltage and waveform diagrams of an M.I. of 0.9 and 0.7 are shown in Figs. 6(a) and 7. (a). Fig. The graphs in figures 6(a) and 7(a) show the current

corresponding to the nine-level and seven-level output voltage waveforms, respectively. The rise in voltage is less prominent when M.I. is decreased (V0peak). The FFT inverter power spectrum is shown in Figures 6(b) and 7 at different M.I values (b). The V0 peak of 361 V is recorded when modulated at 0.9 and the "Total Harmonic Distortion (THD)" is 16.6 percent. The increase in THD can be attributed to a drop in output voltage levels in Figs. 6(b) and 7, which can be regarded as a consequence of the M.I. reduction (b). The outgoing waveform harmonics spectrum is given in Figs. 6(c) and 7. (c). The THD is about 0.5 percent, and the modulation is 0.9 with an I0peak value of 6.4 A. Similarly to the voltage, the I0peak value decreases M.I. The I0peak is recorded at 5.0 A, and the THD is observed to be around 6%.

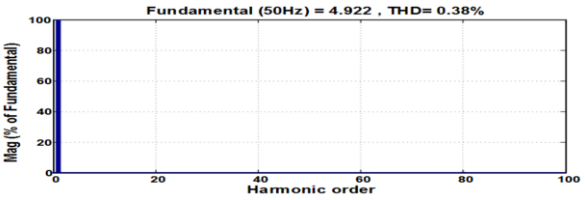
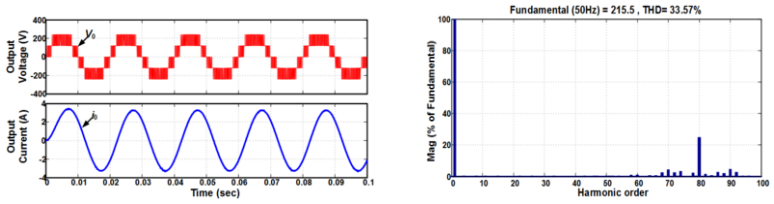
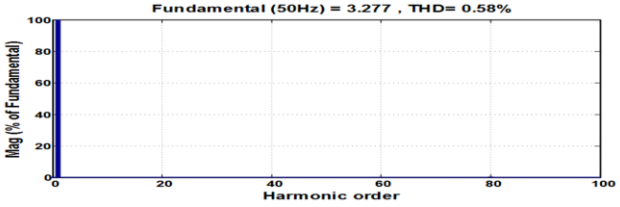


Figure 6. Simulation results of FFT examination of I_0.



(a) **(b)**



(c)

Figure 7 Simulation results at *M.I. = 0.7*: (a) Structure current and voltage wave-form at the results, (b) FFT study of V_0, and (c) FFT investigation of I_0.

5. Conclusion

This paper provides a novel symmetrical PWM inverter circuit using a minimum number of devices to produce the seven-level output. The proposed system is one of the members of the most widely popular group of single dc source-based type MLI configuration family of seven-level DC-AC converters. The employment of single dc source along with several other types of inverters is the most efficient combination to optimize the number of components of a certain inverter arrangement in recent times. The full analyses and modes of operation were offered for zero, positive and negative levels. The presence of some of the lower frequency operating switches result in reduced

losses and enables more efficient setup. The effective and simple sinusoidal PWM is used to produce the pulses needed. The MATLAB/SIMULINK configuration results are verified at 0.9 and 0.7 index levels. The THD waveforms contents are substantially lower than the standard limitations when the FFT output voltage spectrum and the output current are traced.

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