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The Journey of Logarithm Multiplier: Approach, Development and Future Scope

G. Anusha[a], K. C. Sekhar[b,1], B S Sridevi[c], Nukella Venkatesh[d]

[a,b]*Department of ECE, Aditya College of Engineering, Surampalem, India*
[c,d]*Department of ECE, Aditya Engineering College, Surampalem, India*

Abstract In the digital signal processor, IoT, image process and network systems power are more consumed. To avoid this problem there must be effective in hardware applications like area, less power consumption, accuracy in output, speed, and error. Overall, the basic need is the low power requirement. Most of the 3-D graphics are because of multiplication and division. To develop efficiency in hardware logarithm multiplier is the best solution. It is excellent in processing multiplication operations. So that it is maintaining a crucial role in different applications from the past years. But it is a lack to explain complete history in development. Hence, this paper finalizes the complete development steps, involvement performance, and complete error analysis. It is for technical issues, LNS is used majorly. The overall importance of LNS is explained. Error calculation techniques such as antilogarithmic converters, VHDL, and logarithmic approximation are used. The usage of different techniques like Mitchell's approximation and iterative pipeline architecture is to design the hardware components. This paper gives the best result to future designers.

Keywords: ANN, Logarithm multiplier, VHDL, VLSI, IC

1. Introduction

A logarithm is nothing but it involves a bunch of rules to which a particular task should be performed. A multiplier is an operation in which every variable is applied to a logarithm function generator, and after that the generated outputs are combined each other and applied to a function generator of exponential, to get a required output which is proportional to the product of two inputs [1, 2, 3, 4]. The logarithm multiplier is used in many applications it is an important arithmetic component for many applications. But it does not give the literature process on development history briefly in the past. This paper gives the implementation and evolution with a systematic order. Logarithms are also used in the process of speech, scientific calculations, graphics made in computers and artificial neural network operations [2, 5, 6, 7, 8]. Additionally, HDC has been found to be useful in the solving of sequence prediction problems, particularly when the making procedure is a Markov of limited orders with a higher bound that is known to be accurate. Sensor-based Internet of things applications that address such concerns include body sensing and manufacturing liability isolation [9, 10, 11, 12, 16]. Body-sensing devices and data are the most effective applications for emergency medical equipment and data. With regard to machine learning and deep learning algorithms, HDC gives the greatest

[1] Corresponding Author, K. C. Sekhar, Department of ECE, Aditya Engineering College, Surampalem, A.P., India, India; E-mail: sekhar_maddirala@aec.edu.in

outcomes. The HDC backend of the vision engine enables robots to perceive in real time via active perception [13, 14, 15, 17].

For the development of HDC, the key duties will be profiling on conventional and generic architectures, CPU and GPU profiling, as well as language recognition and translation [16, 18]. An integrated circuit is a microchip, it works as a microprocessor, timer, oscillator, amplifier, or even storage element. An IC is a very small chip which is made up of silicon it may bear several transistors, resistors, and capacitors anywhere. The microchip (IC) is playing an important role in the digital domain for the real-time signal process. This is known as digital signal processing. It involves huge arithmetic operators. 86 percentage of the data processing time in three-dimensional graphics is only because of multiplication. Multiplication is the main resource and limiter which is effectively used in DSP and image processing. Logarithm number system (LNS) is an arithmetic system that is majorly used in fixed point (FXP) and floating point (FLP) number system multipliers [19, 20, 21, 22]. This logarithmic multiplier converts multiplication and division operations respectively into addition and subtraction operations.

The calculation of multiplication in logarithmic takes three steps: (1), Logarithmic conversion of binary numbers for logarithmic representation, (2) performing of arithmetic operations in logarithmic domain, (3) last conversion of anti-logarithm [1].

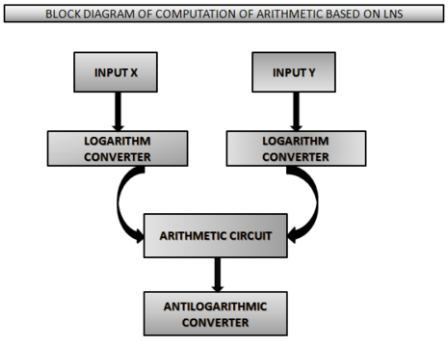

Figure 1. Block diagram representation of Log and antilog converter

2. Literature Review

In 1991, lookup algorithms for fundamental functions and its error analysis paper were published by PT P Tang. In this, lookup algorithms are implemented. These are helpful to calculate the fundamental functions. These are very superior and the best one which gives accuracy when related to other algorithms. This table looks up gives many advantages when compared to others. It is very fast and requires less time and less work. So this method is used in hardware to design the components without the errors [1]. The binary logarithms computation paper was published in 1991 by Demetrios and K. Kotsiopoulos. In this, the calculation of simple algorithms is shown. Simple algorithms like base 2 to base N. This calculation is done step by step and bit by bit process. This is the absolute method for the calculation of simple algorithms. This method can be easily developed in simple with less code [2].

Hardware implementation for precisely rounded fundamental functions paper were published in 1994 by MJSchulte and E Swartzlander. These hardware components are

designed with accurate results for the functions. For designing they use a polynomial approximation in which it produces terms. To reduce these relations the input interval is separated into parts that are equivalent with a dissimilar coefficient [15]. After this adjustment rounded results for all inputs are obtained. This results in less time, area and power [3]. In 2007, implementation of the elementary function for logarithmic number systems paper is published by K. Johansson et al [14]. In this paper there are four elementary functions to realize or to calculate the logarithmic number systems. Approximation method and transformation are used to reduce the time, power and area [4].

A storage efficient tables and additions method for precise calculation of fundamental functions paper was published in 2013 by J.Y. L. Low and C.C. Jong. In this paper, IATA was proposed [13]. Because using tables and additions method there is a huge memory requirement but it is fast and accurate in the calculation. By using this IATA method, it consists of three techniques it is used to minimize the memory requirement [12]. This gives high storage effectiveness than the tables and additions method and also it delivers a large space for exploration [5]. A low power logarithmic number system addition/subtraction and their impact on digital filter paper were published in 2013 by I. Kouretas et al. In that they introduced the techniques for low power dissipation and impact of the evaluation of this technique logarithm number system on digitals. In this, they used to avoid unwanted switching to reduce power [6].

An error analysis of hardware logarithm approximation methods for low power applications paper was published in 2015 by Alicia Klinefelter et al. In this paper there are methods to solve the errors by approximation error method and Mitchell's algorithm method [10]. And also, these methods are used to reduce the time complexity and power [11]. With these advantages, the designers can get satisfied and accuracy output. Finally, these methods are used to design low power applications [7]. An effective VLSI architecture for antilogarithmic converter by means of the error rectification method paper was published in 2016 by Durgesh Nandan et al. In this high-performance antilogarithmic converter and VHDL is used to design the hardware applications effectively by using two region bit level by minimum error cost. Due to effectiveness in hardware the power, area, and time are saved. By using this method there may be a very good result in the future if they design hardware components [8].

An effective VLSI architecture for iterative logarithmic multiplier paper was published in 2017 by D Nandan et al. In the digital signal and image process, the logarithmic number system plays a crucial role. This digital signal processing and the remaining process needs a lot of arithmetic operation. Multiplication is the main operation that is majorly consumed in hardware implementation [9, 10]. To avoid this Mitchell's algorithm with a unified pipeline method is used. Using this technique consumption is less and error cost is effective [9]. An effective antilogarithmic converter by using 11-regions error rectification scheme paper was published in 2017 by Durgesh Nandan et al. In this logarithmic operation by using eleven region bit level is the best solution for the hardware implementation rather than the binary arithmetic operations. By this operation, the area, time, and power are made effective with error cost by using algorithmic converters in hardware applications [10]. In 2018, the logarithm multiplier paper is published. It is the best solution and efficient for hardware. It is a fast multiplication operation [16, 17]. In past years arithmetic is important but there is no brief explanation of development history. In previous publishers, the authors had investigated in logarithm multiplier but they partially concluded that. Hence this paper

gives the development, design, techniques, and advantages of the logarithmic multiplier in brief and systematic literature [11].

3. Design Approach: Logarithm number system

The logarithm number system is used to overcome the technical issues obtained by the binary number system during multiplication operation [14]. When compared to remaining operations multiplication is the most power consuming and area consuming module. Using this system in DSP and image processing may not give the required result. The raised problem can be done by the LNS [13]. LNS has the potential to bear this problem and it uses normal weighted numbers. LNS plays a crucial role in DSP, image process and a neural network system. Digital signal process applications have a main aim to process fast with good hardware performance. LNS multipliers offer benefits over fixed-point and floating-point multipliers in terms of speed and accuracy [15, 18].

Arithmeticians have used logarithms to clarify the multiplication, division, etc., so addition and subtraction can be used to perform such operations. LNS multiplier pieces of advice native data type two families they are fixed-point and floating-point data. Fixed point multiplication is a faster and easier algorithm. It is majorly used in the normal digital process. It gives a clear and better understanding. The floating-point is used in decimal notations to constitute the non-integer numbers.

In the past 1980s, floating-point was implemented and standardized by IEEE experts with two sets one is with 32 bit and another is with 64 bits. And IEEE formats two sets for LNS one is single and another is double precision [16]. The below Table 1 shows the example with two LNS arithmetic operation variables they are Log A and Log B and Log C this variable represents the A, B and C values.

Table 1: Logarithmic Arithmetic Operations

Binary Operation	Logarithmic Operation
C = A*B	log C = log A + log B
C = A/B	log C = log A – log B
C = A+B	log C = log A+ $log_2(1 + 2^{(log\ B - log\ A)})$
C = A-B	log C = log A + $log_2(1 - 2^{log\ B - log\ A)})$

Logarithmic multiplication is generally classified into two types. They are (1): lookup table based (2): Mitchell's Algorithm (MA) based and improving MA Accuracy. And further, the MA is divided into four parts one is (1) divided approximation (2) MA-based iterative algorithm (3) correction term based and last (4) operand decomposition. This lookup table and Mitchell's works are based on interpolation. This requires read-only memory to store the coefficients which are needed. The work of research is applied to the repeating decimal techniques to save the hardware cost but in the cost of speed by performing the conversion method.

4. Results and Discussions

For accuracy and proper design, I studied recent papers that are proposed by D. Nandan, J. Kanungo, and A. Mahajan. The work was completed according to the accuracy and hardware complexity. The error analysis is also calculated between the average error percentage and the maximum possible error.

Table 2. Error analysis

Method	Average (%)			MPE (%)
	4 Bit	8 Bit	16 Bit	
MA^4	------	3.77	3.83	~12
$OD-MA^{26}$	1.441	1.449	2.170	11.11
$\mathbf{Iterative}^{27,28,29}$ $\mathbf{ECC_S}(=0)$	--------	8.913	9.412	25
$\mathbf{Iterative}^{27,28,29}$ $\mathbf{ECC_S}(=\mathbf{1})$	-------	-------	------ ---	6.25
$\mathbf{Iterative}^{27,28,29}$ $\mathbf{ECC_S}(=\mathbf{1})$	--------	--------	------ ---	1.56
$IOD-MA^{30}$	1.6279	1.678	2.064	11.11

This Table 2 shows the average error percentage for 4-bit, 8 bit and 16 bits. This table shows the values of MA, OD-MA, ITERATIVE, and IOD-MA. IOD-Mitchell's approximation for 4 bit is 1.6279% and for is 1.678% and for 16 bit is 2.064 these all are average error percentage. The maximum possible error percentage for IOD-Mitchell's approximation is 11.11%. The average error percentage of OD-Mitchell's approximation for 4 bit is 1.441% and for 8 bit is 3.77% and for 16 bit is 3.83%. The average error percentage of Mitchell's approximation for 8 bit is 3.77% and for 16 bit is 3.83%. The maximum possible error percentage for Mitchell's approximation is nearly 12. The maximum possible error percentage for iterative 27, 28, 29, are 25%, 6.25%, and 1.56%.

5. Applications

Logarithm multipliers are applicable everywhere in real-life scenarios. Some of these applications are discussed in this paper. They are LNS, mathematical circuits, and approximate calculation. Firstly, LNS is used to overcome the technical issues raised in hardware applications. Secondly, an approximate calculation is used in the processing of videos, signal processing, and transmission lines. Mathematical circuits are one of the methods which have more power consumption, large area, and time complexity. To overcome these problems LNS is effectively used.

6. Conclusion

In this paper, the applications, performance, techniques of LNS are discussed. And also the implementation and representation of LNS are said here. Logarithm multiplier, antilogarithm multiplier, and iterative logarithm multiplier techniques are used. I concluded that the iterative method is more effectively worked when compared to other methods. This method is a good inaccuracy that we need in hardware applications. Previously in 2016 Akhter et al partially concluded about the logarithm multiplier. But in this paper, there is a complete analysis of the logarithm multiplier.

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