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Stochastic Computing Solutions Challenges and Application

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Abstract. High speed and power are required for modern applications, and low power consumption and a small integration area. So, this system will be consumed less power. To manipulate these problems either way of computing should be changed by another technique or the transistor should be changed by another device. One selective computing is stochastic. While loaded computing contributes high hardware cost, high speed. Stochastic computing accuracy is less than binary computing circuits. They are having some implementation basic operations of stochastic computing. They are complementary operation, multiplication operation, addition operation, subtraction operation, and division operation. These operations having some logic gates i.e.., AND gate, NOT gate, XOR gate, an XNOR gate. And implement the hardware Tripartite synapse. It can be divided into parts. They are Astrocyte, Synapse, Input spiking, LIF neuron, and output spiking. Using stochastic circuits and conversion processes, this paper demonstrates the fundamental notions of stochastic computing. implementation of arithmetic operations and hardware tripartite synapse and tripartite synapse hardware architecture.

Keywords*:* Stochastic computing, XNOR gate, SDP, Image processing, Tripartite synapse

1. Introduction

Image processing classifiers, for example, have become more difficult and energy-intensive in recent years as a result of technological advancements. That is why it is referred to as a likelihood. Stochastic computing is one sort of approximation computing [1, 2, 3]. It will help you save money on your energy expenses if you use it. Two organizations have collaborated to develop stochastic computing separately [4]. A "bit stream," or a succession of bits, is used in stochastic computing. Small size, low power, accuracy, and high error tolerance are all advantages of stochastic computing [5]. The main advantage of stochastic computing is that it allows for the creation of complex arithmetic operations. Slowness, sloppiness, and lack of precision are all disadvantages of stochastic computing [6, 7]. To create the bit stream in probabilistic computing, a Stochastic Number Generator (SNG) and Comparators (RNG) are used.

The logic gates used in stochastic computing are AND and NOR gates. There are two ways to express stochastic numbers. There is just one power supply for each format.

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As a numerical representation for [8], there existed just (0 to 1) and (-1 to 1) in both formats. Binary computing has a much wider range of applications than stochastic computing. However, the stochastic circuits also suffer from long processing and accuracy degradation. In stochastic computing, complex circuits can be replaced by simple logic operations.

In stochastic computing, many Stoc hasting Number Generators (SNG) are required for higher input bits [9]. The Stochastic Number generators are large due that it occupies the maximum area in stochastic computing. In unipolar and bipolar format, the operation of addition is performed by a multiplexer [10]. Due to the nature of stochastic computing, the sequence of numbers cannot be greater than one. There are two alternatives to operate the delayed version of the input signals. They are converting the input into a stochastic bitstream and the input signal first passes through the delay line [11].

2. Literature Review

In 1992, the methods of data-parallel broadcasting are developed by considering the advantages of properties of nonlinear, stochastic, continuous-time dynamical systems. The stochastic components contain Poisson and Gaussian random white noise. This paper presents to demonstrate that broadcasting can be performed efficiently [12, 13]. In1998, Reactive programmers respond to their environment by altering their behavior. In these programmers, the subsequent inputs are not self-contained. This paper describes such programmers and failures using a stochastic approach. Finally, it may be said that this distribution can be approximated by an exponential distribution [14]. In 2002, stochastic logic was renamed stochastic computing to reflect the new name's more precise connotation. It's fault-tolerant, and it has a minimal physical footprint, which is nice. This process is encoded using Bernoulli random sequences. This study demonstrates that noise can be reduced in the silicon area without changing the basic system structure when utilizing a unified design technique with a parameter [15, 16, 17, 18, 19].

In2017, power grid operation is a term used to describe how electric vehicles and renewable energy are becoming more prevalent. Stochastic models of large-scale energy resources are proposed in this paper in two stages. The results show that the proposed technique outperforms the deterministic model [20]. In 2018, modern applications demand lightning-fast performance and minimum integration. Transistors are getting smaller as technology progresses, making it possible to cram more transistors onto a single chip. As transistor size decreases, leakage current increases, resulting in higher power usage. These problems can be avoided by substituting other devices for the transistor. One technique to computing is stochastic computing. This research [21] illustrates the basic concepts of stochastic computing and stochastic circuits. Spiking neural networks have self-repairing tripartite synapse capability, which was demonstrated in 2019. It's a particular kind of electronic circuit used in hardware. Developing an efficient hardware design is necessary because of the complexity of the tripartite synapse. This study presents a stochastic computing-based hardware architecture that is both efficient and low-cost. Stochastic computing is used to replace complex hardware devices such as DSPs [22].

3. Methodology for Hyper-Dimensional Computing

Conversion Blocks: If you want to use stochastic reasoning, you'll need to transform binary numbers to their corresponding stochastic numbers and vice versa. A comparator and a random number generator are both included. These two functions are included in the block's probability distribution function:

$$fX(\mathrm{x}) = \begin{cases} \frac{1}{2\mathrm{n}} & \text{for } 0 \leq \mathrm{X} < 2^{\mathrm{n}} \\ 0 & \text{for } \mathrm{X} \geq 2^{\mathrm{n}} \end{cases} \quad (1)$$

$$FX(x) = P(x < b) = \begin{cases} \frac{b}{2^n} & for\ 0 \leq b < 2^n \\ 1 & for\ b \leq 2^n \end{cases} \quad (2)$$

Pulse to binary converter consists of a simple counter. The output of this block is given as

$$PN(X) = \binom{N}{X} . \mathrm{P}^{\mathrm{X}.(1-\mathrm{P})^{\mathrm{N\_X}}} \quad (3)$$

In stochastic computing, these blocks are more costly than actual processing circuits. Block diagram for pulse binary converter is given as in figure 1:

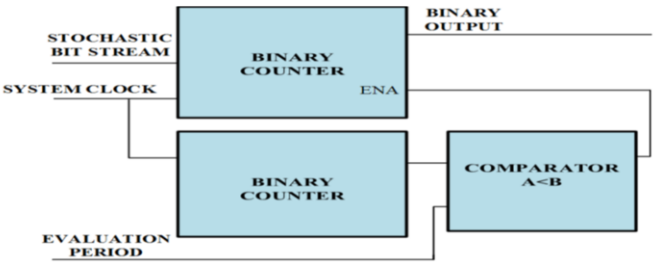

Figure 1. Block diagram for pulse binary converter

Stochastic Bitstream means stochastic computing signify numbers as streams of random bits and regenerates numbers by calculating frequencies. A binary counter is a digital circuit consists of clock input and several count outputs which gives the number of clock cycles. The output may vary either on falling or rising clock edges. A comparator is a device for comparing an object with a similar object or with a standard measure shown in figure 3.

The complementary operation, in this operation, using a simple NOT gate to implement unipolar and bipolar format. Multiplication operation, in unipolar format, is achieved by using a AND gate and in bipolar format, it is achieved by using an XNOR gate. Division operation, Stochastic division operation contains up/down counter, comparator, XOR gate, and AND gate.

3.1 Optimized tripartite synapse: The tripartite synapse consists of three parts. They are Astrocyte, Synapse, and Neuron. A simplified tripartite synapse structure is shown below in figure 2.

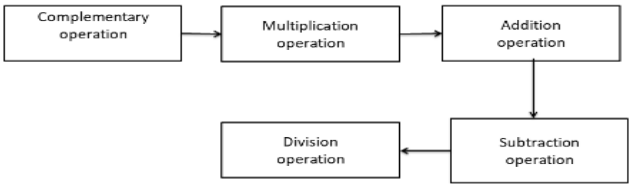

Figure 2. Arithmetic operations in stochastic implementation

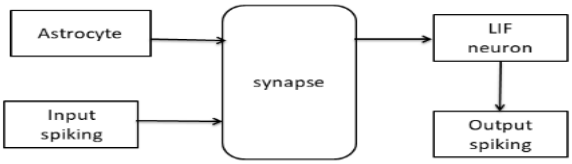

Figure 2. Optimized tripartite synapse

Synapse is the site of carrying electric nerve impulses between two nerve cells or between a gland and a neuron or muscle cell. Astrocytes are a species of glial cells in the central nervous system. They are also recognized as astrocytic glial cells. Spiking is the membrane potential reaches the threshold, the neuron will heat, and make a signal that excursion to other neurons which, decrease or increase their potentials in return to this signal. LIF neuron is a Leaky integrate and fire neuron, it represents a parallel combination of leaky capacitor and resistor. In the synapse model, when the PR is high, the current is produced and injected into the neuron. When the membrane potential is greater than the threshold selected neuron, an output spiking is produced in the neuron component. The synapse is given as,

$$I_{syn}^{i}(t) = \begin{cases} I_{inj,} rand \leq PR \\ 0, rand > PR \end{cases} \quad (4)$$

The mostly used LIF neuron model is given as,

$$\tau_m \frac{dv}{dt} = -v(t) + R_m \sum_{i=1}^{m} I_{syn}^{i}(t) \quad (5)$$

Tripartite synapse hardware architecture: The data range of stochastic computing is [-1, 1] it does not reach the tripartite synapse model calculations. So the data range is extended. It is extended from [-1, 1].

4. Implementation Technique

Stochastic computing is a technique to implement complex functions at a low cost. Stochastic computing works in different number formats. The number format

travels through stochastic designs with high accuracy, less power consumption, and less complexity. Figure 1 shows the Block diagram for the pulse binary converter. It consists of a Stochastic Bitstream, System clock, Binary counter, Evaluation Period, Comparator, and Binary output. Figures 3 (a) and (b) shows the Stochastic implementation of basic arithmetic operations. It consists of Complementary operation, Multiplication operation, Addition operation, Division operation, Subtraction operation. Complementary operation is using simple NOT gate to perform the unipolar and bipolar format.

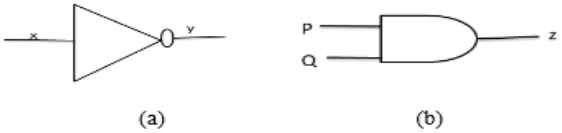

Figure 3. (a) NOT gate(b) AND Gate

In addition, operation, both in the unipolar and bipolar format it is operated by a multiplexer. The sum of two inputs is the output, not the absolute sum. These two inputs are obtained in UESL and SESL shown in multiplexing operation in shown in figure 4.

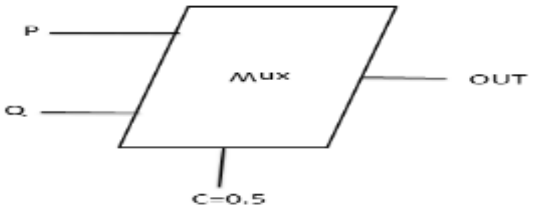

Figure 4. Multiplexing operation

Subtraction operation is developed by a single XOR gate in unipolar format. The gate inputs should be correlated. The output should not be the actual difference. It should be the absolute difference inverter and multiplexing. Division operation, contains up/down counter, comparator, AND gate, an XOR gate. The hardware needed division operation in the comparator, AND gate and XOR gate formats are enough more than UESL and SESL. It is accomplished by two XNOR gates and two AND gates. The optimized tripartite synapse consists of three parts. Synapse, astrocyte, and neuron. In this model whenever the PR is high the current is developed and injected into the neuron. Output spiking is developed in the neuron component whenever membrane potential is higher than threshold neuron shown in figure 5.

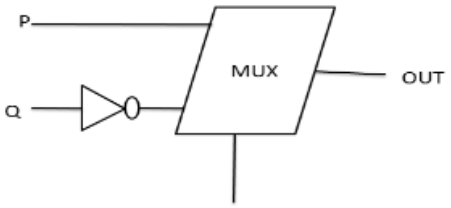

Figure 5. Multiplexing inverter operation

5. Conclusion

Stochastic computing is used to reduce the lime and minimization of cost. In conversion blocks, it is required to convert binary digits into their corresponding binary number. In this probability density function and distribution function for the block and block diagram for a pulse, the binary converter is addicted. And basic arithmetic operations are used with the logic gates and multiplexers. The hardware tripartite synapse is implemented. It has some blocks and tripartite synapse hardware architecture is accustomed. We introduce many FSM-based stochastic computational elements in this research, and demonstrate how to use them to create four basic digital image processing algorithms. According to our experiment, stochastic computing systems have a strong resistance to soft errors. It doesn't matter if the clock is running slightly late or slightly early. Another significant benefit of stochastic computing is that the critical path is short, meaning that clock frequencies can be pushed even higher. Stochastic computing, as contrast to conventional computing, uses significantly fewer resources and yields the same output. Future work will concentrate on the construction of a programmable, stochastic computational architecture for digital signal processing, and the investigation of more stochastic computational elements built on FSM.

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