

Assertion Driven Modified Booth Encoding and Post Computation Model for Speed MAC Applications

S.Sivasaravanababu ^{a,1}, T.R.Dineshkumar ^a, Dr.G.Saravana Kumar ^a

^aAssistant Professor, Department of Electronics and Communication Engineering, Vel Tech High Tech Dr.Rangarajan Dr.Sakunthala Engineering College, TN, India

Abstract. The Multiply-Accumulate Unit (MAC) is the core computational block in many DSP and wireless application but comes with more complicated architectures. Moreover the MAC block also decides the energy consumption and the performance of the overall design; due to its lies in the maximal path delay critical propagation. Developing high performance and energy optimized MAC core is essential to optimized DSP core. In this work, a high speed and low power signed booth radix enabled MAC Unit is proposed with highly configurable assertion driven modified booth algorithm (AD-MBE). The proposed booth core is based on core optimized booth radix-4 with hierarchical partial product accumulation design and associated path delay optimization and computational complexity reduction. Here all booth generated partial products are added as post summation adder network which consists of carry select adder (CSA) & carry look ahead (CLA) sequentially which narrow down the energy and computational complexity. Here increasing the operating frequency is achieved by accumulating encoding bits of each of the input operand into assertion unit before generating end results instead of going through the entire partial product accumulation. The FPGA implementation of the proposed signed asserted booth radix-4 based MAC shows significant complexity reduction with improved system performance as compared to the conventional booth unit and conventional array multiplier.

Keywords. Multiply-Accumulate Unit (MAC), assertion driven modified booth algorithm (AD-MBE)

1. Introduction

The advent of High speed communication in 5G devices high performance arithmetic modelling is the key and heart of next generation applications to build unified accumulation and multiplication units that are optimized can be utilized in many applications such as finite impulse response (FIR) filtering , Fast Fourier transform (FFT) computation and wavelet transform etc. parallel prefix accumulation is widely preferred for many digital signal processing (DSP) and wireless communication devices for improved system performance. It is also used for formulating extended arithmetic units such as multiplication and division unit. To narrow down path propagation delay and design complexity overhead in adder unit many works introduced various prefix topologies. In most cases, the notable performance degradations occur with input bit

¹ S.Sivasaravanababu, Assistant Professor, Vel Tech High Tech Dr.Rangarajan Dr.Sakunthala Engineering College, TN, India; E-mail: sivasaravanababu@velhightech.com.

width of the adder unit. In general many DSP applications need to accommodate large number of multiply and accumulator (MAC) operation and its hardware accumulation are also increased accordingly [1].

2. Related Works

Many previous works focused only on FIR filter design optimization using various multiplication methods like booth, Vedic for high performance and canonical sign digit (CSD) formulation [2] of filter coefficient for low complexity. However, the major issues with these models are that, as the complexity reduced the performance rate is also significantly degraded; or vice versa. Therefore, unified model is required to narrow down this performance gap.

To accomplish this task, in recent years many works has been investigates the prefix accumulation and DA arithmetic for complexity reduction, high throughput and low power FIR design. Researchers also investigate the booth for various DSP applications since FIR design based on residue arithmetic offers both high speed as well as optimized computational complexity overhead. The architectural choice of FPGA provides additional metrics in RNS systems due to its resource availability. Technology-dependent hardware optimizations for FPGA implementations of FIR filters are implemented in [3]. Here improved performance is archived by realizing 4:2 compressor and carry save adder (CSA) multiplication for different types of FIR filter architectures such as direct form, Transposed form and Hybrid form. The optimization also includes efficient post mapping using 6-input LUTs in addition to the hardware realizations. The hardware realizations process includes modification of design strategy and module instantiation within each boolean networks.

In [4], parallel prefix structures are used to suggest a novel signed-digit-to-canonical-signed-digit recoding. Some CSD models re-code from 2's complement binary numbers, while the presented CSD architectures convert from signed-digit numbers. Here each digit associate to the input is accompanied by its sign. The evaluation shows that the proposed CSD model with the conditional sum configuration outperforms current CSD models by 30%.

To solve this problem, the DA-driven reconfigurable block-based FIR filter architecture proposed in [5] used a modular DA scheme that could handle larger block sizes and longer filter lengths. Here the memory space requirements are not increase linearly with the filter order. In comparison to standard ones, the proposed approach provides 8 times the high-throughput reconfigurable FIR filters.

In [6] presented a detailed analyzes of various hardware efficient FIR design approaches. The decomposition of LUTs into small sub groups offers significant complexity reduction in DA LUT FIR structure. However, the degree of parallelism and FIR order continue to increase the complexity accumulation proportionally.

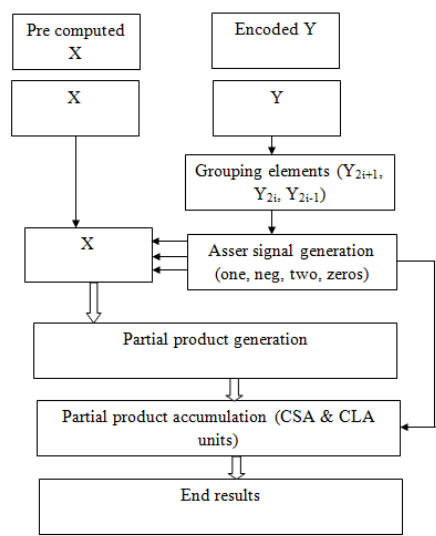


Figure 1. Proposed modified booth radix model

$A * B = 123 * 10$
01111011 * 10
011 110 11 0
Grouping
011 111 101 110
2X 0 -X -X
PP = 000010100 000000000 111110110 111110110 = 1230

3. Proposed Assertion Driven Booth Algorithm

Among various path delay reduction and hardware sharing-During partial product accumulation CSA adders were reused (hardware sharing). In case of zero signals asserted that associated PP generation & accumulation can be skipped (Digital Transition reduction). and also used CLA for last two rows of PP addition for reduced path delay overhead as shown Figure 1. Full of parameterized model – for reconfigurability which can configured dynamically. Two complements circuit insertion- to support both signed and unsigned multiplication.

- Since it can cut the number of partial items in half, the radix-4 booth algorithm is used to boost multiplier efficiency.
- In radix-4 , we consider 3 bits at a time as shown in Figure 2.

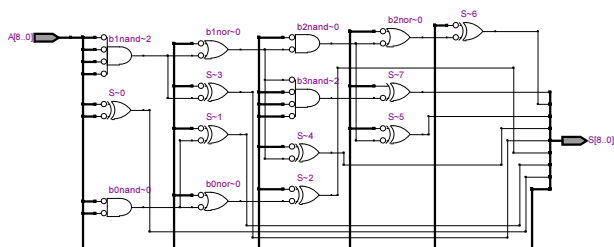


Figure 2. Schematic model of radix encoding model

3.1 Assertion methodology

This function involves transformation of booth encoded values into control signals which comprise of bitwise Exclusive-OR operation between input and a encoding state array as follows:

- Zeros – for avoiding PP generation and associated PP accumulation
- Twos – enable associated shifting operation ($2X$ is equal to $X \ll 1$) that can be done during PP accumulation.
- Negs - to allows inversion and 2's comp units
- Ones – no changes required

3.2 Advantages of proposed BOOTH MAC System

High Performance: The absence of multiplier components during MAC arithmetic results in high speed computation.

Energy efficiency: To realise the MAC method, regardless of the order input operands, only a single accumulator portion is used, which minimises the digital transfer activities during MAC operations. Switching events that are 1-0 or 0-1 are directly proportional to power. This will simplify the overall architecture by regulating the arithmetic accumulation.

4. Experimental Results

4.1 Simulation Results

To prove the value of assumption in the partial product generation process and its effect on the MAC machine during the multiplication process, suitable test inputs are used at different stages of data propagation, as shown in Figure 3. The potential benefits of optimal PP generation and its efficiency over conventional booth MAC design is also proved through simulation results

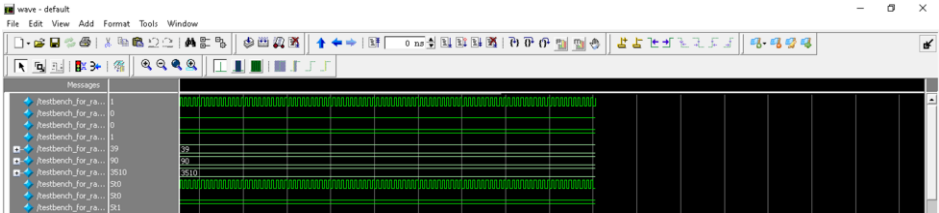


Figure 3. Booth simulation results with unsigned input

4.2 Hardware synthesis results

In this chapter, we compare the performance metrics of proposed modified booth over conventional encoding based booth radix-4 model and validated the metrics both in terms high performance and complexity trade off measures. For state-of-the-art contrast, the proposed booth radix-4 core is modelled using Verilog HDL and synthesised using FPGA QUARTUS II EDA synthesiser. The resultant MAC is capable of achieving a flexible tradeoff with least possible design complexity and tolerable energy efficiency .Moreover, by exploiting the benefits of PP computation which can minimize memory space requirements and can able to support the path delay optimization using the CSA and CLA model. In this asserted booth radix-4 can able to jointly optimize the computational complexity and energy from beneficiary tree enabled PP computation.

Table 1. Performance comparisons between modified asserted booth MAC model using FPGA hardware synthesis results

MULTIPLIER MODEL	Design complexity(LEs)	Speed(MHz)	Total Power dissipation (mW)
Array multiplier	327	129.57 MHz	103.08mW
Booth radix-4	285	244.02MHz	101.73mW
Proposed booth radix-4	261	255.43 MHz	100.02mW

4.3 Performance comparison report

The FPGA hardware synthesizer tool has been used to measure the power utilization report and its experimental results are listed in Table 1. From the logical elements utilization summary it is proved that the proposed modified booth using asserted booth arithmetic model offers 20% area efficiency over conventional booth radix-4 approach and achieves 3% power consumption reduction. The energy efficiency of optimized PP transformation is also proved to be the significant one as shown in Figure 4 through FPGA hardware synthesis results.

PowerPlay Power Analyzer Summary	
PowerPlay Power Analyzer Status	Successful - Tue Mar 30 02:23:28 2021
Quartus II Version	9.0 Build 132 02/25/2009 SJ Web Edition
Revision Name	TOPG
Top-level Entity Name	booth_radix4_algorithm
Family	Cyclone III
Device	EP3C5F256C6
Power Models	Final
Total Thermal Power Dissipation	100.02 mW
Core Dynamic Thermal Power Dissipation	10.99 mW
Core Static Thermal Power Dissipation	46.18 mW
I/O Thermal Power Dissipation	42.85 mW
Power Estimation Confidence	Low: user provided insufficient toggle rate data

Figure 4. Power dissipation report

5. Conclusion

Here in this work hardware implementation of assertion driven modified booth radix-4 algorithms with all forms of partial product transformation and analyzed its performance metrics. It is also demonstrated that assertion unit introduced for booth algorithm offers significant energy level optimization and open a platform for low applications. Here, we propose a hierarchical tree based PP addition along with assert signal extraction model as a path delay optimization scheme that provides least critical path both at encoding and end stage. Here we proved that modified assertion based booth will give better hardware complexity and power optimization with considerable delay enhancement.

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