

# Enhanced and Efficient Carry Select Adder with Minimal Delay

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**Abstract:** In today's digital world, Arithmetic computations have been evolved as a core factor in digital signal processors, micro-controllers, and systems using arithmetic and logical operations such as adders, multipliers, image processors, and signal processors. One of the elements that play an important role in performing arithmetic calculations is an adder. Among many adders, the Carry Select Adder produces less propagation delay. However, there may be an increased delay, power consumption, and area required in the case of a normal Carry Select Adder. To overcome the mentioned drawbacks, an improved model of Carry Select Adder has been designed that uses Binary to Excess – 1 Converter. Instead of using multiple blocks of Ripple Carry Adders (RCAs), it is efficient and effective if one of the blocks is replaced with Binary to Excess – 1 Converter. As a result, we can achieve a high speed adder with minimal delay, minimal power, and reduced area.

**Keywords:** Bit enhanced, Minimal Delay, Carry Select Adder (CSLA) and Binary to Excess – 1 Converter (BEC).

## 1. Introduction

VLSI circuits with high speed and minimal delay are a core part of this technological world. The performance and efficiency of a circuit are in the hands of adders and multipliers which is the deciding authority in VLSI design [1-4]. In carry select adder there is a trade-off between ripple carry adder and carry look ahead adder in area and delay [5]. Low power and Minimal delay circuits play a vital role in many VLSI-based systems, Digital Signal processors, Generic processors, and Complex Arithmetic and Logical units. The role of adders has become inevitable in every digital circuit. An Adder that has been widely used for its fast processing feature is the Carry Select Adder (CSLA). Even though many works have been done on Carry Select Adder, yet a minimal effort has been taken to enhance it by bit-wise, and to reduce its delay. In keeping this as a central theme, a proposed carry select adder has been modeled which operates on 256 and 512 bits of binary data with minimal delay and providing efficient results at a faster rate. The binary addition is the most fundamental arithmetic operation that is most often used. In maximum designs, add end as play a critical role and operating speed. [6].

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Carry selection adder is one of the quick adders because it overcomes the problem of transport propagation by having two probable carry values. (i.e., both  $c_{in}=0$  &  $c_{in}=1$ ). Carry select adder uses ripple carry adders and multiplexer. Hence propagation delay comes into consideration. In ripple carry adder, carry propagation causes delay. To increase the efficiency of an adder, a new approach is presented in this paper. To overcome this delay a code converter is used. The code converter unit reduces delay, area and power utilization. Hence we can achieve greater speed.

## 2. Existing Carry Select Adder (CSLA)

Ripple Carry Adder (RCA) delivers the most compact design, but takes more time to calculate. Time-critical apps utilize Carry Look-ahead. [7] A Conventional Carry Select Adder (CSLA) has two Ripple Carry Adders (RCAs) and Multiplexers is shown in figure 1. For the addition of two n-bit numbers, two RCAs are multiplexed together and addition is performed. For example in the case of adding two 4-bit numbers, two 4-bit ripple carry adders perform the addition with carry-in being 0 at one time and carry-in being 1 at the other time. After the carry-in is known by calculating addition, correct sum and multiplexer selects the correct carry. The performance of large digital circuits is dependent upon the speed of the circuits that make up the different functional units. Adders are among the most widely used. [8]. The bit number given to the Carry Select blocks can either be static or dynamic. For static case, the computational delay is of the order of  $O(\sqrt{N})$ , where N refers to the number of bits provided at the input to a Carry Select Block. For dynamic case, the delay can be calculated by the number of multiplexer chains. As a result, the delay varies with respect to the number of multiplexer blocks utilized.

In carry select adder we have two ripple carry adders and multiplexers. Adding n bit of two numbers is done by two adders (RCA) one with  $C_{in}=0$  and the other with  $C_{in}=1$ . Based on the carry that propagates at each stage from one bit to the other bit, the multiplexer selects values between two carry values. With different adders, Ripple Carry Adder is straightforward to layout however consumes more postprocess for the reason that convey little bit of closing complete adder is legitimate simplest after the joint propagation delay of all complete adder cascaded [9]

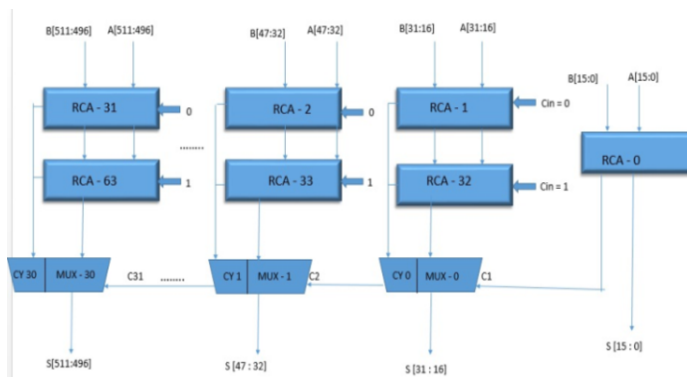


Figure 1. Existing 512 Bit CSLA

### 3. Enhanced Carry Select Adder (E-CSLA)

The designed new model of Carry Select Adder in figure2 is enhanced both in terms of Number of bits that it can process as well as the delay that it encounters during the computation. The proposed adder is being capable of processing 256 and 512 bits of data, one at a time. Despite the rise in bit number, computation can be done with a vast binary data compared with normal carry select adders. As a result, the proposed adder is more effective in doing computations in processors ranging from generic to Digital Signal processors. [Bit enhanced].The delay is significantly reduced in this method. Because of BEC the area occupied by this enhanced CSLA is greatly reduced. The speed is also increased which makes the arithmetic calculations faster. Hence this enhanced approach can be utilizes in many applications.

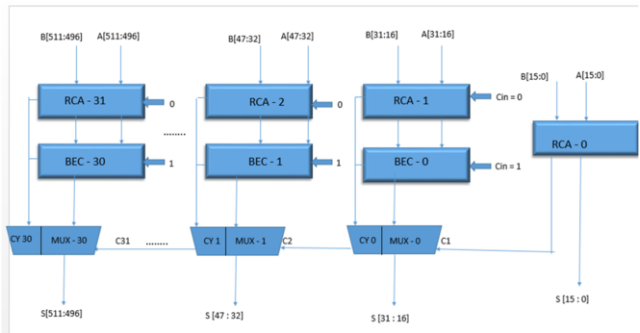


Figure 2.Enhanced 512 Bit CSLA (E-CSLA)

This adder varies from existing Carry Select Adder by using Binary to Excess-1 Converter (BEC) instead of a Ripple Carry Adder (RCA). Because of using BEC, one can effectively reduce the propagation delay and as well reducing the computational time. As a result the area that it uses while fabricating it to an IC in processors is significantly reduced to an extent. The RTL schematic in figure3 of the enhanced CSLA is given below.

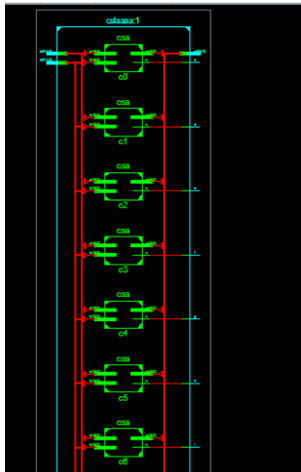


Figure 3.RTL schematic

#### 4. Comparisons

From the table 1, it is obvious that the proposed Carry Select Adder ensures a minimal delay compared with other adder circuits.

**Table 1.**Delay Comparison Table

VARIOUS TYPES OF ADDERS	DELAY (in ns)
Ripple Carry Adder(RCA)	28.741 ns
Carry Look Ahead Adder(CLA)	24.196 ns
Carry Select Adder Without BEC(CSLA)	20.035 ns
Carry Select Adder With BEC(E-CSLA)	18.689ns

In addition to the proposed work, research based on comparisons of few existing adders is also undertaken. The various existing adders are already elaborated in the papers [10].A few adders are taken and simulated with the help of Xilinx version 14.7. The comparisons are tabulated in the table 1. The listed delay is for 512 bit. Our proposed work is for 16, 32, 64, 128, 256 and 512 bit. Although the number of bits increased in a wide scale we achieve greater speed, low power utilization, low area and minimal delay in our work.

#### 5. Future Enhancements

This modified approach can also be enhanced to many bits. Also, this work can be implemented with image enhancement for digital signal processing, and it can be achieved with the help of MATLAB. The image enhancement can also be a successful implementation of this proposed work. Besides image enhancement FIR filters, integration and some mathematical operations can be carried out which will have a great scope in emerging digital industry. In the rapid growing digital technology image enhancement will have numerous application by using this proposed system of design of an adder with binary to excess 1 converter unit.

#### 6. Results of Simulation and Discussions

The existing design and the new designed model for various sets of inputs are coded and executed with the help of Xilinx tool version 14.7.the test bench program for different sets of inputs are executed and verified. The below figure 4 and 5 display the simulation results of the modified adder. The comparison of adders also are simulated and verified for their delay and other parameters check. Thus the simulation results and

its RTL schematic diagram are illustrated below. Thus our proposed modified adder achieves less delay with greater speed.

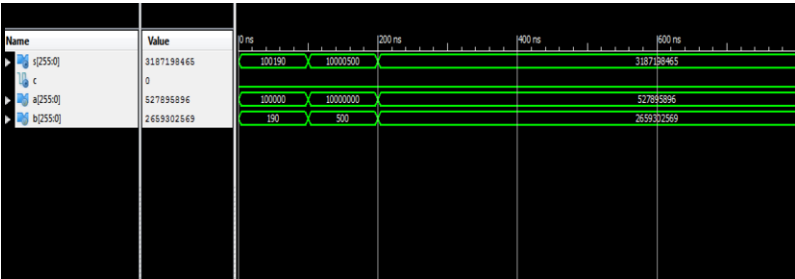


Figure 4. Simulation Result of 256 Bit

7. Conclusion

Thus the new designed system of Carry Select Adder offers minimal Delay with increased number of bits, Binary to Excess-1 Converter for reducing the computational time. Therefore this adder occupies lesser area and utilizes lesser power compared with Conventional Carry Select Adder. This design is implemented in FPGA kit and simulated in Xilinx software. This new designed approach can be used in many applications like arithmetic calculations for speedier results.

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