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A Contemporary Survey on Low Power, High Speed Comparators for Bio-Medical Applications

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Abstract. The analysis of biomedical signals performs an important role in figuring out numerous issues in clinical science. Also, the urge to track biomedical signals in fitness and well-being control is progressively growing with the multiplied occurrence of persistent sicknesses over the last decade. By nature, the most of the real-time signals are analog. Hence, an Analog to digital converter (ADC) is required to transform the signal. In ADC architecture, the comparator is the essential block that performs a vital role and consumes greater power in ADC design. Numerous architectures for comparators relate to biomedical programs are mentioned in recent days. In this paper, the exceptional latest techniques of comparator designs are discussed with their key capabilities in conjunction with pros and cons.

Keywords. Low power and high-speed comparators, Latch, preamplifier, DC, offset voltage, dynamic power.

1. Introduction

Implantable medical devices (IMD) are commonly battery-operated and fairly energy-constrained. Replacing an implant is not advisable for the reason that surgical treatment is risky and high-priced too. The importance of battery-operated devices with less weight, small size, and low power paves to design ultra-low-power ADCs. During a previous couple of years, diverse strategies were delivered to help the reduction in supply voltage and power dissipation in Bio signal processing systems. The continued scaling of feature size is often essential to improving the battery life of the medical implant device. There are 3 major demanding situations influence low voltage operation: 1. In submicron technology, the device parameters such as feature size together with the length of the channel (L), the thickness of gate oxide (tox) are continued to scale down which results in reduced supply voltage to make certain device

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reliability. 2. Due to growing the variety of additives on a single Si chip dissipates a quantity of power according to unit area results in over-heating. Overheating of a chip is avoided only by less density in order that the power of the digital circuit desires is restricted. 3. The next challenge is associated with the battery-powered system. Due to portability and to have proper functionality, the supply voltage, and supply power need to be decreased [14]. The energy consumption of comparators has an enormous impact on the whole energy intake of the device. Hence, the design of low power and high-speed comparator is needed to perform the necessity of responsibleness. Fundamental blocks present in SAR ADC are depicted below [5]:

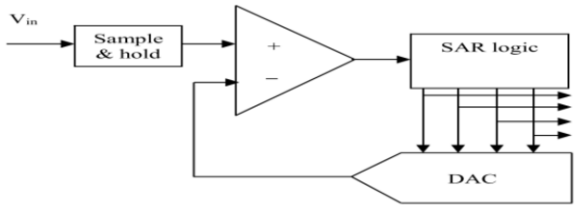


Figure 1. SAR ADC architecture

SAR ADC is one of the most suitable candidates for bio signal process applications among all [13]. It includes Sample and Hold Circuit, Comparator, SAR Logic, and DAC Module. The Comparator is the one, consumed up more power nearly 70% within the complete architecture. Hence, optimizing the overall performance of the comparator on the premise of its figure of merit is relatively important.

2. Literature Review

Comparator is a vital part of Analog to Digital Converters (ADC) withinside the mixed-mode signal designs. Numerous Researches are illustrated with different circuits and strategies to improvise the performance of comparators. The dynamic comparator has high input impedance, negligible static power consumption, rail-to-rail output swing, precise noise, and mismatch robustness, consequently, it's far pretty distinguished for SAR ADC in Ref. [1],Kasi Bandla, et.al, has reviewed that static power consumption is excessive in Dynamic Latch Comparator with Pre-Amplifier topology and consequently no longer most suitable for low power applications. However, the above-mentioned topology is ideal for correct evaluation the Charge Sharing Dynamic Latch Comparator (CSDLC) is used in order to have low energy. Also found that it fails to offer rail-rail output swing in each of the clock cycles. They additionally observed; the one another topology called Strong-Arm Dynamic Latch based comparator (SADLC) is used to clear up the troubles. They highlighted its overall performance with other different comparator topologies in Ref. [2].

As another example, in Ref. [3] mentioned by G. Murali Krishna et.al, has reviewed the design of dynamic comparators, in comparison with traditional comparators and Double tail comparators. They proposed a design that includes a P-MOS latch which ensures predictable delay throughout an evaluation segment. Another segment reset is similar to a traditional comparator. The above-stated topology is controlled via way of means of a unique clock signal designed cautiously to consumes much less power. They also added that the speed of the comparator will increase the use of input NMOS transistors.

Parvin Bahmanyar et.al, in Ref. [11] has discussed the performance of a double-tail latched comparator designed for ultra-low-energy applications. This method is well-perfect for Low supply voltages among four hundred mV to one V and also self-neutralization and reduction in kickback noise are key features of this technique. In general, the proposed circuit achieves a good figure of merit, the results are in comparison with a traditional double-tail latched comparator. In this method, large gain amplifiers are used to attain the proper resolution due to this bandwidth of the Amplifier has got reduced consequently affects the gain bandwidth trade-off.

The comparator mentioned in Ref. [6] has mentioned the design withinside the sub threshold region to have a very low energy intake that's appropriate for SAR ADC. They also noted that an adjustable calibration capacitor array is used in the design to cancel the charge error caused by parasitic capacitors. The proposed comparator may be operated at a supply voltage of 0.75 V and an overall energy intake of 250 nW received as a result. It is proven in Ref. [7] The low-offset dynamic comparator is another promising design proposed for low-power applications. It ensures good performance in the aspect of lesser power and offset voltage. An approach mentioned right here is to use the tail transistor with careful sizing which ends up reducing the energy intake in dynamic comparators in Ref. [7].

As discussed in ref. [8], the proposed comparator and controller are more suitable for Implantable Medical Devices. The method proposed in Ref. [9], High-speed dynamic analog comparator that gives low offset and no longer requires any preamplifier. A four-input dynamic comparator is mentioned by Chi-Chang Lu and Ding-Ke Huang in Ref. [4]. In this method, the twin sampling process is used throughout the sampling segment because the applied input signals are multiplied by factor two for every instance. As another example in Ref. [5] Ahmed Naguib et.al, have developed a model precise for Energy-Efficient Biomedical SAR ADCs and mentioned static energy lifestyles throughout the amplification segment.

3. Comparator Topologies

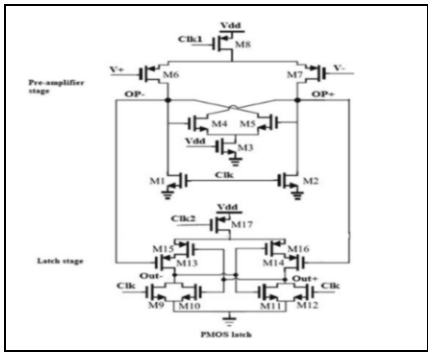
This section deals with the prevailing few comparator architectures that have been mentioned within the literature overview. In this paper, we also speak the merits and demerits of each mentioned comparator topology with respect to their figure of merits.

3.1. Comparators

They are referred to as 1-bit converters and commonly used in analog to digital converter. In the A/DD D conversion process, the analog input to be sampled at the earliest then applied to an aggregate of comparators to decide its digital value. In preferred, Comparator consists of the preamplifier level, latch, and output amplifier called Buffer. The preamplifier is needed to acquire sufficient gain on the way to save the input offset voltage of the dynamic latch. The usage of a separate preamplifier does not find in some ADC designs due to the fact that the CMOS latch itself performs the amplification. The latch/ selection module is one of the essential blocks it needs to be capable of discriminating mV range signals. It's formed by an input differential pair that imbalances a pair of crossed-coupled inverters, growing wonderful remarks that boost the outputs to the rails which result in proper decision [10]. The very last thing

inside the comparator layout is an output buffer or post-amplifier that helps to transform the decision output into a logical signal (i.e., 0 or 1 V).

3.1.1 Conventional Comparator



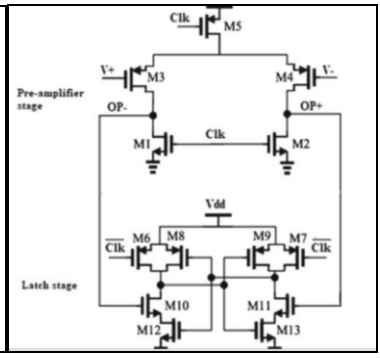
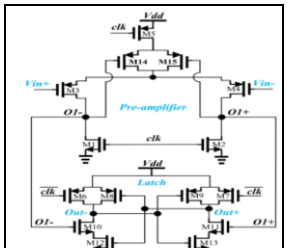
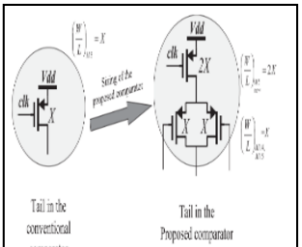


Figure 2. Conventional dynamic Comparator **Figure 3**. PMOS Latch Comparator

This comparator is constructed with the useful resource of a pre-amplifier and latch. It has stages of operation named, reset, and evaluation phase. In the conventional circuit, large parasitic capacitors are created at nodes during the course of an evaluation phase, which observes high energy consumption, and a larger time is needed to finish the whole process. P-MOS latch comparator has proposed to solve all the mentioned issues. It produces predictable delay within the course of the evaluation stage whereas the delay was unpredictable and uncontrollable within the conventional comparator. The reset segment is similar to a conventional comparator. The proposed topology is controlled with the aid of a unique clock signal generated cautiously. In the P-MOS latch, the size/dimension of M4, M5 transistors needs to be taken care of to enhance the differential gain.

3.1.2 Low-power dynamic comparator





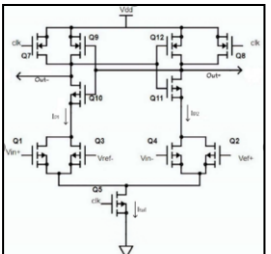


Figure 4. Low Power dynamic Comparator **Figure 5.** Tail transistor sizing **Figure 6.** Strong Arm dynamic latch

In this approach, tail transistors (M14, M15) are small in size added with traditional low offset dynamic comparator to improve the performance, as an end result, energy overhead is significantly negligible (less than 10%). Due to the tail current, the output

swings completely to reach the full-scale value near V_{dd}-$|V_{thp}|$, which reduces leakage power.

3.1.3 Strong-arm dynamic latch comparator

As static power dissipation is immoderate in Dynamic Latch Comparator consequently not suitable for low power applications. The method illustrated here in Fig.6. used two clocked nMOS tail-transistors and in preference with transistors Q1, Q2, Q3, and Q4 are re-arranged in comparison with dynamic latch, this method helps to resolve static power leakage and enhances other figures of merit.

Table 1. Comparisons of different Topologies for Bio Medical Applications

Topology used	Avg Power consumption	Offset voltage	Frequency	V_{dd}(V)	Area (μm^2)	Speed @ Vcm 0.9 V	Technology
Conventional Comparator	556 µW	2.65 mV	0.5 GHz	1.8 V	343 μm^2	1.16 GHz	0.18 µm
Tailed Comparator with Transistor Sizing [7]	347 µW	2.19 mV	0.5 GHz	1.8 V	361 μm^2	1.05 GHz	0.18 µm
Relative Observation	+37.6%	+15.8%			-5%	-9.5%	

Topology used	Total Average Power (µW)	Operating Frequency	Supply Voltage (V)	Maximum power (µW)	Delay	Technology
Conventional Comparator	1.87	0.5 GHz	5	154	350 pS	250 nm
Double Tailed Comparator	3.78	0.5 GHz	5	122	500 pS	250 nm
PMOS Latch comparator	1.25	0.5 GHz	5	115	250 pS	250 nm

Topology used	Average Dynamic Power (µW)	Offset voltage in (mv)	Supply Voltage (V)	Clock-Feed-through	Kick Back Noise	Average Delay in (ps)	PDP (fJ)	Technology
CSDLC	18.0	63	1.8	0.04	0.216	178.1	3.2	0.18 µm
SADLC	4.82	6	1.8	0.059	0.182	92.75	0.447	0.18 µm
Strong Arm Dynamic Comparator	4.72	6	1.8	0.06	0.184	93.4	0.44	0.18 µm

4. Conclusion

Bio physiological signals are low voltage and low-frequency signals. Hence, analysis requires a converter with low noise and low power operations which helps to extend

the lifetime of the battery-powered bio-implants. In this aspect, various types of dynamic comparators have been discussed and shown in Table 1. From the above table, we found that the performance of the comparators differs with respect to design methodology primarily supply voltage and simulation type. The authors also observed that the double tail comparator with proper transistor sizing, Strong Arm Dynamic Comparator, and ultra-double-tail latched comparator operated within the voltage swing between 0 to 2 V are suitable for SAR ADC on Biomedical applications. We have planned to adopt hybrid adiabatic energy optimizing logic to implement a double-tail latched comparator since there is a lot of scopes available for further energy optimization.

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