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Low Power, High Speed MUX Based Area Efficient Dadda Multiplier

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Abstract. The multiplier is a fundamental building block in most digital ICs' arithmetic units. The multiplier architecture in modern VLSI circuits must meet the main parameters of low power, high speed, and small area requirements. In this paper, a 4-bit multiplier is constructed using the Dadda algorithm with enhanced Full and Half adder blocks to achieve a smaller size, lower power consumption, and minimum propagation delay. The Dadda Algorithm-designed multiplier is used in the first phase to reduce propagation delay while adding partial products in three stages provided by AND Gates. In the second phase, each stage of the Dadda tree algorithm is built with an enhanced Full and half adders to reduce the design area, propagation delay, and power consumption while still meeting the requirements of the current scenario by using MUX logic. In an average of Conventional array Multipliers, the proposed Dadda multiplier achieved an 84.68 % reduction in delay, 70.89 % reduction in power, 84.68% increase in Maximum Usable Frequency (MUF), and 95.55% reduction in Energy per Samples (EPS).

Keywords. 4*4 multiplier, Dadda algorithm, Enhanced Full and Half adder, MUX logic

1. Introduction

The multiplier is used in a variety of applications, including VLSI design, signal processing, digital communication, and electronics. In the current scenario, low power, high speed, and a small area are important. Multipliers with the least delay and power dissipation are chosen in order to achieve optimal throughput and device response when designing an optimal circuit. The Dadda Algorithm multiplier architecture operates at a high frequency and consumes comparatively less power, as well as magically reducing power consumption, which leads to the concept of using it in larger circuits where multipliers play a major role [11-12].The Dadda Algorithm-designed multiplier is used in the first phase and MUX logic in the second phase, each stage of the Daddatree algorithm is built with an enhanced Full adder and half adder to further reducethe design area, propagation delay, and power dissipation. This paper has sevensections. Multiplier with an existing method is presented in Section II, proposed research is described in Section III, block diagrams and algorithm implementation are

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presented in Section IV and V, simulation and implementation results are listed in Section VI, and the conclusion is in Section VII.

2. Previous Research

Many algorithms named Wallace tree [1-2], Vedic and Booth algorithms [3] were used in previous research to achieve optimized power and delay product. To reduce the area and latency, a booth encoding method was used in conjunction with a compressor [4]. Furthermore, to minimize switching operation, partial products [5] are reordered to reduce power consumption. In the reduction power, a modified full adder with 4:1 multiplexers is used, and a full adder with six 2:1 multiplexers is also designed. The digital design with low power dissipation and minimal delay, as well as maximum throughput and high speed can be achieved byvarious techniques such as merged delay transformation [6], genetic algorithm [7], evolutionary algorithm [8], delay path Un-equalization [9], carry-look-ahead logic [10], etc.

3. Proposed Research

To achieve less area, low power consumption, and minimal propagation delay, a 4-bit multiplier is constructed using the Dadda algorithm and enhanced Half and Full adder blocks in the proposed work. The multiplier built in the first phase with the Dadda algorithm was used to reduce the propagation delay. By using multiplexer logic, a multiplier built in the second phase uses enhanced Full adder and half adder to further reduce the design area, propagation delay, and power dissipation. Area is saved as a result of the above two steps, and propagation delay is magically reduced.

3.1 Introduction to Dadda Tree Algorithm

A 4*4 multiplier has 16 partial products, the tree's height is four. The Dadda Algorithm was used to reduce the tree's height from four to two levels. Since the simulation of the next stage does not need to wait for carry from the previous stage, the Dadda Algorithm is ideal for reducing the overall multiplier design delay.

3.2 Dadda Algorithm Stages

The aim of the algorithm is to reduce the tree's height from four to two. The height of the tree is reduced from four to three in the first stage and from three to two in the second stage of the Dadda algorithm. By using ripple carry adders in the third stage of the Dadda algorithm, the tree's height is limited to two. To reduce this tree, the first two Dadda stages are used. The Dadda phases are depicted in Figs. 1, 2, and 3.

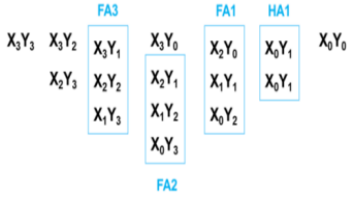

Figure 1.First Stage of Dadda Tree

Figure 2.Second Stage of Dadda Tree

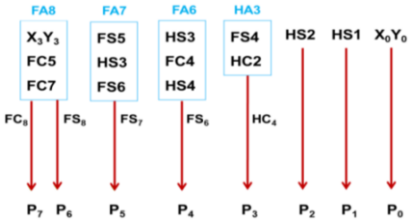

Figure 3.Third Stage of Dadda Tree

3.3Algorithm Implementation

To minimize the height of the tree from four to three, a half adder is added to the second column, a full adder to the fourth column, and two full adders to the third and fifth columns. To reduce the height of the tree from three to two, two half adders are applied to the third and fifth columns, and two full adders are applied to the fourth and sixth columns in the second level. In the final step, ripple carryadders are used to confine the multiplication results. Parallel processing of half adders and full adders, where each adder works independently and does not wait for carry from the previous level, will increase the efficiency of the implementation.

4. Architecture of Proposed Dadda Multiplier

The block diagram of Proposed Dadda multiplier is shown in Fig. 4.

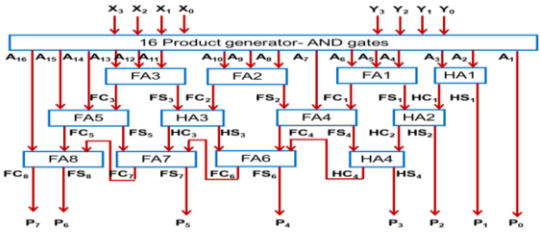

Figure 4.Block Diagram of Proposed Dadda Multiplier

5. Building Blocks of Proposed Multiplier

The MUX-based enhanced AND gate, enhanced half adder and enhanced full adder are shown in Fig.5,6 and 7 respectively.

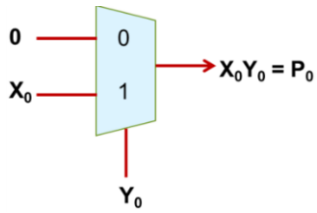

Figure 5.Proposed AND gate using 2:1 MUX

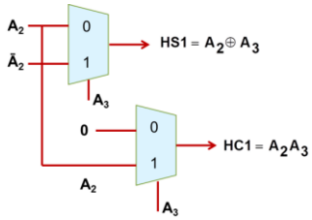

Figure6. Proposed HA using 2:1 MUX

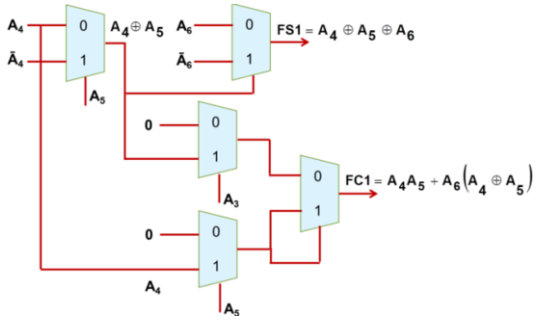

Figure 7. Proposed FA using 2:1 MUX

6. Implementation Results

This section describes the implementation results of a four-bit multiplier based on the Dadda algorithm, as well as enhanced full and half adders. Using Altera Quartus II and the EP2S15F484C3 device, a four-bit multiplier design is developed and simulated. Table 1 shows the design, implementation, and analysis of a multiplier using enhanced full adders and half adders, as well as their performance parameters. The RTL view, Chip layout and simulation output of the proposed multiplier are shown in Fig.8, Fig.9and Fig.10, respectively. The proposed Dadda multiplier with enhanced full adder and half adder achieved 84.68% reduction in delay, 70.89% reduction in power consumption, 84.68% increase in Maximum Usable Frequency (MUF), and 95.55% reduction in Energy per Samples (EPS).

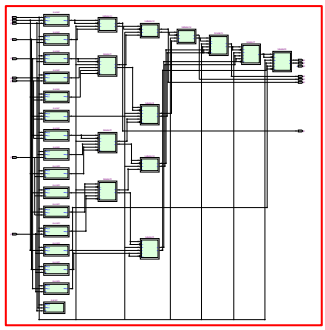

Figure 8.RTL View of Proposed design

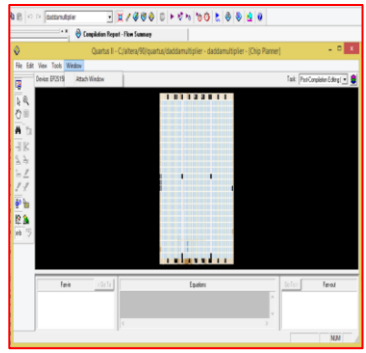

Figure 9. Chip layout of proposed design

Figure 10. Simulation Output of Proposed Design

Table 1. Performance Comparison

Multiplier Type	Delay(ns)	Power(mW)	MUF (MHz)	PS (ns x mW)
Multiplier using Conventional Full Adder	49.98	2.197	20.00	109.8
Multiplier using 4:1 MUX based Full Adder	49.09	5.592	20.37	274.5
Multiplier using 2:1MUX based Full Adder	49.57	1.218	20.17	60.37
Proposed Dadda Multiplier using 2:1 MUX	7.588	0.6	131.78	4.5528

7. Conclusion

The proposed 4 bit multiplier design has been developed, and the schematics have been simulated using Altera Quartus II and the EP2S15F484C3 unit. The schematic for the

Dadda tree algorithm is shown, which includes an AND gate with a 2:1 MUX, a half adder with two 2:1 MUX, and a full adder with four 2:1 MUX. The output parameters are compared to those of current full adder array multipliers. As the proposed design incorporates the Dadda algorithm to minimize propagation delay and the number of stages or area of the multiplier, it is implemented efficiently. Furthermore, by enhancing the full adder and half adder in each stage of the Dadda tree algorithm, in an average of Conventional array Multipliers, the proposed Dadda multiplier achieved an 84.68 % reduction in delay, 70.89 % reduction in power, 84.68% increase in MUF, and 95.55% reduction in EPS.

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