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Design and Performance Analysis of Low Power High Speed Adder and Multiplier Using MTCMOS in 90nm, 70nm, 25nm and 18nm Regime

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Abstract. Nowadays, VLSI technology mainly focused on High-Speed Propagation and Low Power Consumption. Addition is an important arithmetic operation which plays a major role in digital application. Adder is act as an important role in the applications of signal processing, in memory access address generation and Arithmetic Logic Unit. When the number of transistors increases in system designs, makes to increase power and complexity of the circuit. One of the dominant factors is power reduction in low power VLSI technology and to overcome the power dissipation in the existing adder circuit, MTCMOS technique is used in the proposed adder. The design is simulated in 90nm, 70nm, 25nm and18nm technology and then comparison is made between existing and proposed system in the context of energy, area and delay. In this comparison, the efficiency metrics power and delay are found to be reduced 20% from the existing adder and the proposed adder is used for the design of low power multiplier.

Keywords. Multiplier, Adder, Power Consumption, VLSI Technology, Low power, (MTCMOS) Multi-threshold Complementary Metal Oxide Semiconductor

1. Introduction

In digital systems, some kind of digital circuits are largely used to execute addition of figures. It also forms the basis of division, multiplication and subtraction. Addition is the basic operation for analyzing any digital systems discussed in [3]. Power utilization increases, as no of transistor increases. So, the primary needs in the VLSI design are low power design. For emerging low power and high-speed IC fabrication, the deep submicron technologies are used as challenging criteria analyses in [4].From our references, hybrid adder model is one of the heuristic approaches for power reduction with less transistor counts. For our literature survey, in [12] analyzed numerous adders with performance parameters are achieve the numerous areas, power and speeds

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necessities for implementation. Researchers mainly focus to plan a well-organized arithmetic circuit that one works with greater speed and low power in the Power rakishness mainly hang on the substituting action, wire and node capacitances along with size of the control circuit [2].Full adder is one of the fundamental digital circuits that make addition. Full adders are executed with logic gates in hardware. There are two types in full adders they are static and dynamic full adders [5]. Static adder has no static power dissipation, rail to rail swing, the speed of the circuit relied on the transistor sizing and different parasitic that are involved in with it and the signal been swings in static adder all the way to supply [19]. Voltage levels are both the positive and negative rails, no invariable potential dissolution. The transistor sizing and different dependents that are mixed up in with it's based on speed of the circuit. The issue with is kind of execution is that for N fan in circuit 2N number of transistors are required i.e., more area is wanted to get applied [13].

2. Materials and Methods

From the literature survey, we observed some logic styles with positive and negative side are given below. Dynamic CMOS has a main advantage of increased speed and reduced implementation area [8]. The number of transistors required here are less (N+2) as compared to 2N in the static CMOS circuits. Dynamic logic circuit has less loss in static power. But it needs clock for the proper operation. Based on clock, it consumes more power and more complexity than static circuit. In dynamic CMOS logic certain additional power is spent when the circuit has to precharged after every evaluation [12]. Static CMOS logic is one of the logics, which does not require clock. The output will be as soon as the inputs are probed (without considering the propagation delay of the circuit). This logic is contrast to dynamic CMOS which relies on the temporary storage of signal using various load capacitances [11]. The different logic styles include in static CMOS logic are Pseudo NMOS logic, Broadcast logic and Authorization transistor lucidity etc. The Pseudo NMOS logic can be developed by only one PMOS with always ON condition and N-block for logic implementation [11]. Fast switching operations and less transistor count are the advantages of pseudo NMOS logic. This logic has more static power dissipation due to the use of pull up devices, reduction in voltage levels and gain. These reasons this logic makes more vulnerable to noise. So, the Pseudo NMOS logic gives more speed with less static power consumption than static design of circuits [7].Pass transistor logic narrate the numerous logical operations used in the plan of integrated circuits. By removing redundant transistors, it minimizes the computation transistors used to build different logic gates [14]. It uses few transistors, runs faster; require less power than in CMOS logic. The sum of dynamic plans implemented in pass transistor logic but it has the disadvantages that the dissimilarity of the voltage between high and low logic levels reduces at each phase. Every device in sequence is a lesser amount of soaked at its output then at its input [10]. A commonly raised gate may be essential to replace the signal voltage to the full value, if some devices are connected in sequence in a logic track. By dissimilarity, standard CMOS logic transistors show the output joins to the power supply rails, so that in sequential chain the logic voltage stages does not decreases. This has an impact on capacitance and speed of the circuit. Dynamic adder relies on the temporary storage of signal value on the capacitance. This type also has no static power dissipation and uses a sequence of charging and discharging with the addition of the clock input. The

main advantages of this type are increased speed and reduced realization area. In this article we design a high speed adder using MTCMOS technology. The proposed structure analyzed in various nanometer technologies. The technologies are 90nm, 70nm, 25nm and 18nm technology and to present the comparison is made between existing and proposed system in terms of area, power and delay. In this comparison, the efficiency metrics like power and delay is found to be reduced 20% from the existing adder and the proposed MTCMOS Low power adder. And this proposed design can be implemented in array multiplier circuit.

2.1. Existing method of full adder

The existing full adder circuit is presented by [9] as shown in Fig.1 is comprise of individual 14 transistors and divided into three components. Module 1 represent the XNOR module, Module 2 along with Module 3 represent the Transmission gate Component which generates Sum and C_{out} signal respectively. The XNOR Module is constructed using 6T (6 transistors) to eliminate the threshold voltage drop in the module. This module is built on the cross joined PMOS arrangement, and it correspondingly utilize the cross joined NMOS arrangement to create the pair. For the combination of A=B=0 and A=B=1 are processed by the feedback MOSFETs. The gateway voltage loss connected with circuit is also eliminated. This feedback lowers the maximal operating frequency and when compared with other XNOR gates. It also provides the full voltage swing analyzed in [9].

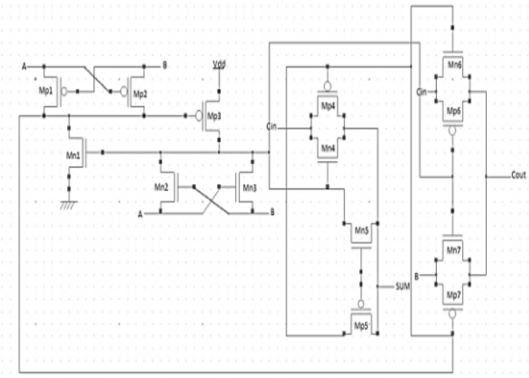

Figure 1. Existing Full adder presented

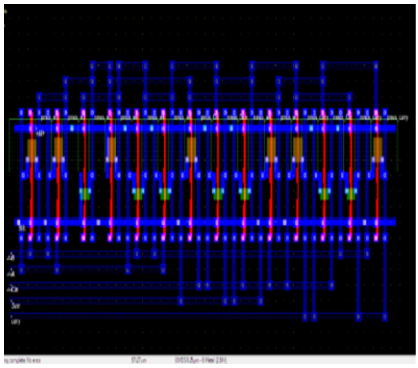

Figure 2. Layout of the existing full adder

The second module sum is constructed and to reduce the power to practicable extends. In this second module XOR gate designed based on transmission gate [6]. The input to this module is given from the output of the first module. This design is not allowed any rail of power or ground. It's a main reason for the absence of short circuit and low power dissipation. But the drawback of this module is not capable of driving bigger loads. The third component is constructed by means of transmission gate logic as shown in the Fig 1. This module is fundamentally a multiplexer which passes either A (or B) or C_{in}, as per the rate of the output of the first module. The input signal A and C_{in} delivers the pouring control for this module, then whichever of the signal will pass. This design is used to avoid lacking power of C_{out} signal in which a key or buffer tracks

the output of the adder cell. In Fig.2 is shown as layout for the existing full adder presented in [10].

2.2. *Proposed method of full adder*

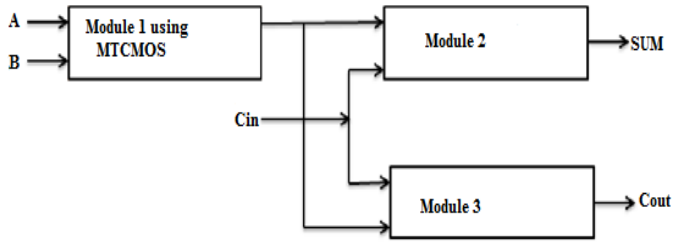

Figure 3. Block diagram of the proposed full adder

The XOR module is still provides power even when it does not give output since it does not produce output for input A=B=0 and A=B=1. This will contribute to the total power consumption of the circuit. In chip design one of the greatest technologies is CMOS which is commonly used today to construct integrated circuitry in numerous submissions. CMOS technology is quite appropriate skill for numerous mechanisms in memories, microprocessors and microcontroller applications. It has negligible static power dissipation. Energy dissipation is an acute parameter in VLSI circuits as a result of systematic shrinkage in dimension of CMOS circuits. Excess power usages in VLSI circuit require excessive wrapping and freezing systems that makes it the cost and reduces the system reliability.MTCMOS is named as Multi-threshold Complementary Metal Oxide Semiconductor. An efficient method to handle power dissipation is scaling the supply voltage. MTCMOS technique is a powerful circuit-level technique which provides low power consumption and high performance by using sleep transistors. This low power technique maintains the circuit efficiency while dropping the sub threshold current in standby mode [13].

An unavoidable thing in VLSI is power management as the automation lies down, so the low-power method should be used to minimize power dissolution. There is multiple origin of power dissipation in digital circuits such as switching activities and short circuit current of the circuit and the other one is due to leakage current. High leakage current is converted into an essential contribution to power dissipation of CMOS circuits [12]. MTCMOS is the low power design which is employed to decrease the power utilization. Generally standby currents, as prime reason of power loss, it can be reduced by using MTCMOS technique [16]. In this approach the use of sleep transistors to increase speed at low supply voltage with low power dissipation.

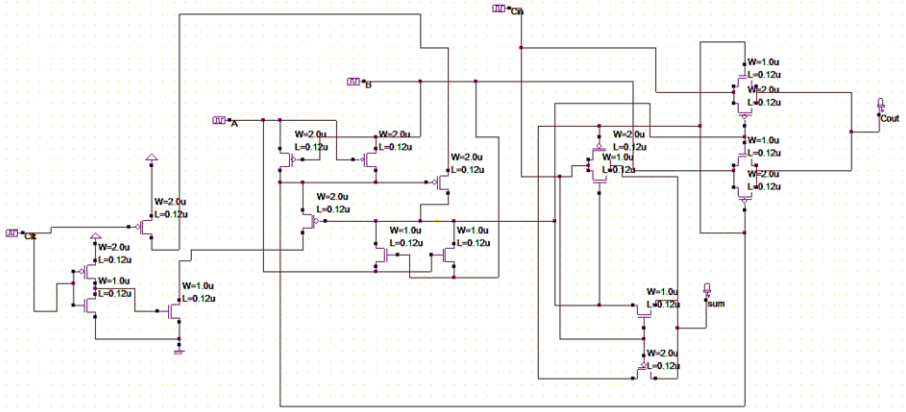

Figure 4. Circuit diagram of proposed full adder

In the submitted plan of adder using MTCMOS technology has 18T (18 transistors with 9 PMOS and 9 NMOS) as presented in the Fig.4. In Fig.3 shows the functional block diagram for the proposed adder. In the suggested design of adder using MTCMOS gives less mean power consumption as estimated to the standard design of circuit. The main reason for the reduction of average power dissipation of the circuit is Sleep transistors. Sleep signals in sleep transistors are used to enable the transistor. In this logic uses two types of threshold transistors with high and low value. In standby mode the High threshold transistors are act as sleep transistor to reduce power consumption. In active mode the Low threshold transistors are used to increase the performance of the circuit. Also High threshold transistor is linked in the middle of logic circuit and power supply. This technique is used to reduce the sub- threshold leakage during standby mode. For low power and high speed applications one of the efficient technique is MTCMOS. The main task during designing a circuit using MTCMOS is sizing of the transistor.

The proposed adder circuit was simulated on SPICE Tool with 90nm, 70nm, 25nm and 18nm technology. The layout for the proposed full adder is done in various nanometer regimes. The performance matrices are taken from the layout of all nanometer régimes. The comparison of MTCMOS technique with conventional technique used in adder circuit in terms of area, power and delay.

3. Results and Discussion

The complete adder strategy in Fig.1 was employed in 90nm, 70nm, 25nm and 18nm by means of SPICE package. Then the transient examination is attained for existing and proposed methods in 90nm, 70nm, 25nm and 18nm regions. The performance analysis of compared with existing systems. Generally power utilization divided into three major types like static, dynamic and leakage power dissipation. Dynamic power dissipation is one of the major reasons for power consumption. In CMOS circuits the Static power dissipation is resulted by leakage and biasing currents. Generally this is lesser than the dynamic power dissipation. It arises due to charging and discharging of load capacitances. In this work we analyze power dissipation in various nanometer technologies. Transient analysis was found for the proposed adder with 90nm and 70nm technology.

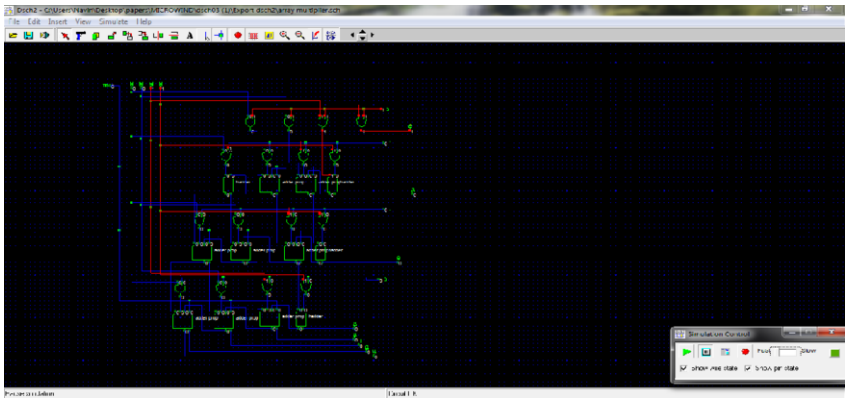

Figure 5. The proposed array multiplier by using the proposed MTCMOS full adder

One of the applications of full adder is multiplier. Multiplier is one the important block in arithmetic logic unit for various operations. It is used in signal processing applications, microprocessor applications and data manipulation function etc. [15]. So today, the design of multiplier with less power is most important role. In this paper to design a multiplier by using the proposed MTCMOS Full adder is implemented in Fig.5 and power, delay are compared. The simulation result for the planned multiplier was found.The comparative results of the proposed adder are given below. The existing adder in [9] is analyzed in 90nm, 70nm, 25nm and 18nm regime. The analysis factors are area, power and delay are done and the parameters are compared to the proposed one. In proposed adder for 90nm technology, the circuit functioned at 0.9v the entire power feasting was recognized to be 18.215µW, for 70nm technology, it was found to be 11.46µW, for 25nm technology, it was found to be 7.78µW and for 18nm technology, it was found to be 3.57µW.The delay is also one of the major parameter in analysis. The delay was found for the proposed full adder in various nanometer technologies are to be 206.78ps for 90nm, 198.07psfor 70nm, and 150.92psfor 25nm and112.23ps for 18nm technology. The adapted full adder is realized in Fig.4. It is recognized that the typical power feasting for the proposed MTCMOS full adder in 90nm technology is 16.64µW, for 70nm technology is 8.21µW, for 25nm technology is 5.23µW and for 18nm technology is 1.72µW. This reduced power feasting is primarily due to nonappearance of outflow current. The comparison is made by various parameters of the proposed full adder and multiplier was compared in Table-1 and Table 2.

Table 1. Comparison matrices for the proposed full adder in various nanometer regimes

Technology	90nm			70nm			25 nm			18nm		
Metric	Area (Sq.m)	Power (µW)	Delay (pS)	Area (Sq.m)	Power (µW)	Delay (pS)	Area (Sq.m)	Power (µW)	Delay (pS)	Area (Sq.m)	Power (µW)	Delay (pS)
Existing [9]	350	18.22	206	140	11.46	198	96	7.78	150	66	3.57	112
Proposed	517	16.64	190	297	8.21	170	210	5.23	130	174	1.72	94

Table 2. Comparison Results of various matrices in existing and proposed Multiplier

Technology	90nm			70nm		
Metric	Area (Sq.m)	Power (μW)	Delay (pS)	Area (Sq.m)	Power (μW)	Delay (pS)
Multiplier using Existing adder	4294	69.244	46	3387	56.739	38
Proposed Multiplier using Proposed adder	5544	39.222	41	4472	36.722	34

4. Conclusion

In this research, a modified Full Adder is executed in 90nm, 70nm, 25nm and 18nm technology. Both the actual and planned Adder strategies were replicated by means of SPICE Tool. It is recognized that the power and postponement is condensed by the usage of MTCMOS technique was found to be for 90nm technology, the circuit functioned at 0.9v the overall power consumption was found to be 18.215μW, for 70nm technology, it was found to be 11.46μW, for 25nm technology, it was found to be 7.78μW and for 18nm technology, it was found to be 3.57μW. Also the power and delay of the proposed multiplier was found 39.22μW for 90nm technology and 36.722 μW for 70nm technology. The Power, Delay and Area of both existing and proposed designs are measured and it is observed that power and delay are minimized in the case of the anticipated adder strategy. The extent of the anticipated adder design is increased. In this comparison, the performance metrics like power and delay is found to be reduced 20% from the existing adder and the proposed adder and is used for low power multiplier.

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