Analysis of Vedic, Wallace Tree and Array Multipliers

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Abstract- Multiplications are the most important and crucial operation in any system. They are done through the process of repetitive addition. Since speed is necessary in any factor therefore multiplication must also be done in a faster way so that they are utilized properly for a faster result. This paper gives a detailed explanation on all three multipliers and compares them accordingly-In this paper, three various multiplication methods are considered and simulated. Three structural multipliers such as Vedic, Wallace tree and array multipliers are compared and their output is shown through the FPGA. For comparison, the results of multipliers are synthesized and simulated using XILINX.ISE.14.5 tool .Later the comparison is concluded by evaluating their utilization of the device.

Keywords -Vedic Multiplier (VM), Wallace Tree Multiplier (WTM), Array Multipliers (AM)

1. Introduction

Multiplication operation plays a very important role in micro processing, DSP and other communication applications. Consider two 8-bit number, From the Figure.1, it can be.

Figure 1. Multiplication process

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observed that multiplication is just a lot of addition involved. Hence these multipliers are designed using full adders and half adders. The multiplier is efficiently built using a compactor to make it suitable for various implementations of speed, low power and compact VLSI [1]. A high-speed, two-complement, m-bit by n-bit parallel array multiplication algorithm is outlined [2]. [3] Introduces a new architecture for the multiplier recoded by radix-2 Booth, where its delete extended sign bits. One of the basic arithmetic operations is multiplication and it takes considerably more hardware resources and processing time than addition and subtraction [4]. It is a good direction to minimize the number of operations, thus reducing a dynamic force that is a big part of total power dissipation, in order to reduce substantial power usage of multiplier nature [5][9-10]. The performance study of the Wallace-tree, Array and Baugh-Wooley multiplier architectures has been carried out [6]. The delay and power dissipation of the Wallace Tree multiplier is lower, while the Array multiplier is better for applications with reduced area but not speed. In [7] a low-power one-bit full adder had been proposed which is used in the Arithmetic Logic Unit configuration. Some strategies that are helpful in minimizing leakage power have been implemented in [8]. An adjustment to decrease the amount of half adders is presented to the reduction of Wallace that guarantees that the delay is the same as for the reduction of conventional Wallace [11]. The design of low-power high-speed algorithms for arithmetic logic units using ancient mathematics techniques and implementing their hardware is proposed in [12]. In this paper, three multipliers are discussed. They are:

1.1. Vedic Multiplier

Vedic multiplier is based on 16 Vedic sutras which describes natural way of solving whole range of mathematical problems. It produces product and sum in a single step. Their calculations are done parallel which makes Vedic the fastest multiplier. As the number of bits increases in a Vedic multiplier the timing delay decreases greatly when compared to other multiplier. The block diagram of VM is shown in Figure 2.

Figure 2. Block diagram of VM

1.2. Wallace Tree Multiplier

Wallace tree multiplier is an efficient implementation of digital circuit is shown in Figure 3. Wallace tree multipliers are considered to perform efficiently but they are hard to implement. Although they are considered to be the faster multiplier than simple array multiplier, they include Partial Product Generation, Reduction and Addition. At first normal operations take place, then the products are generated and secondly the heights of the set of products are reduced to two by placing adders. Once they are reduced to two additions is performed. Here $A = A_0 A_1 A_2 A_3 A_4 A_5 A_6 A_7$ and $B = B_0 B_1 B_2 B_3 B_4 B_5 B_6 B_7$ and the result is given by P.

Figure 3. Block diagram of WTM

1.3. Array Multiplier

The array multipliers are the layout of combinational multipliers is shown in Figure 4. Although it utilizes more gates the performance is easily increased using pipeline technique. The add and shift algorithm is followed in array multipliers. The partial products are generated and shifted according to bit orders and addition operation take place. The result for multiplying two numbers is obtained by using AND logic gate that gives bit of the product .Consider 8X8 bit multiplication with $A= X_0 X_1 X_2 X_3 X_4 X_5 X_6 X_7$ and $B= Y_0 Y_1 Y_2 Y_3 Y_4 Y_5 Y_6 Y_7$ and the result is given by S.

Figure 4. Block diagram of AM

2. Simulation Result

To generate output two inputs are given to a multiplier. A="157"(in decimal number system), B="129"(in decimal number system) Output ="20253"(in decimal number system) which is shown in Figure 5.

Figure 5. Simulation result of the Multiplier

2.1. FPGA Implementation

The final procedure is to implement them in a hardware kit is shown in Figure 6. The result is done in both hardware and software using XILINX. Here initially a0 is in on state (a0=1) and b1 is in on state (b1 =1) and other values set as ‘0’ that will be displayed in data input switches. The output is displayed in LED Indicators. There are 8 LED Indicators.X0 (1) is in on state(X0(1) =1) and others will be in off state. The performance Comparison of Vedic, Wallace and Array multipliers are given in Table 1 and in figure 7.

Table 1. Performance Comparison of Vedic, Wallace and Array multipliers

TYPE OF MULTIPLIER	DELAY (ns)	LUT (used and availability)
VM	27.908ns	126 out of 7168
WTM	31.962ns	131 out of 7168
AM	34.04ns	156 out of 7168

Figure 6. Hardware Implementation

Figure 7. Performance comparison

3. Conclusion

The implementation of 8x8 multipliers such as Vedic multiplier, Wallace tree multiplier and array multipliers are done. It is observed that delay in each multiplier vary respective to their design and hence it is found that Vedic multiplier uses less delay than any other multipliers and considered to be the fastest in its performance. Also the utilization by Vedic multiplier is less than other multipliers. Therefore in this paper it is verified that Vedic multiplier is the most suitable technique to implement complex mathematical problem.

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