New Energy and Future Energy Systems G.L. Kyriakopoulos (Ed.) © 2022 The authors and IOS Press. This article is published online with Open Access by IOS Press and distributed under the terms of the Creative Commons Attribution Non-Commercial License 4.0 (CC BY-NC 4.0). doi:10.3233/AERD220007

Zero-Sequence Circulating Current Suppression for Parallel Three-Level Backto-Back Converters Based on DPWM Hybrid Switching Modulation Strategy

 Mingjin DING^{a,1}, Lei XIE^a, Changyu ZHU^b, Yongmi ZHANG^b and Cheng SHI^c
 ^a Nanjing SAC New Energy Technology Co. Ltd., Nanjing 210000, China
 ^b China Huadian Inner Mongolia Energy Co., Ltd., Hohhot 010000, China
 ^c School of Electrical Engineering and Automation, Harbin Institute of Technology, Harbin 150000, China

> Abstract. A single wind turbine can no longer meet the increasing installed capacity and reliability requirements. Therefore, the power level and stability requirements of the wind power generation system can be improved through the parallel connection of three-level back-to-back converters. However, the zero-sequence circulating current (ZSCC) will distort the three-phase current, increase the power loss and reduce the system efficiency. Therefore, this paper establishes the ZSCC equivalent model of the back-to-back parallel converter, and analyzes the generation principle of the zero-sequence circulating current. In order to reduce the switching loss of the system and increase the system efficiency, a novel DPWM modulation strategy is proposed. At the same time, in order to control the zero-sequence circulating current of the parallel system, a hybrid switching modulation strategy using DPWM1 and DPWM3 based on hysteresis control is proposed. The simulation and experimental results verify the effectiveness of the zero-sequence circulation suppression strategy for the parallel system.

> **Keywords.** Circulating current suppression, three-level back-to-back converters, DPWM, hybrid switching modulation strategy.

1. Introduction

With the large-scale integration of wind power generation systems into the mediumvoltage distribution network, the power grid has put forward higher requirements on the quality of the output current waveform of the full-power grid-connected converter. Due to the advantages of good harmonic performance, low switching loss, high system efficiency, and low electromagnetic interference, three-level converters have been more widely used than two-level topologies [1-3]. The power converters in the wind power generation system usually need to be used in parallel to increase the system capacity, and at the same time, the efficiency and reliability of the system can also be improved.

¹ Corresponding author, Mingjin Ding, R&D Department, Nanjing SAC New Energy Technology Co. Ltd., 8 Xinghuo Road Pukou Hi-tech Region, Nanjing, China; E-mail: mingjin-ding@sac-china.com.

Financial supports from the S&T Major Project of Inner Mongolia Autonomous Region in China (No. 2020ZD0018).

However, the parallel connection of converters will generate a zero-sequence circulating current path, which will lead to circulating currents between converters, which will increase system losses, cause grid-connected current distortion, and affect the service life of switching devices [4-6]. In the parallel system of three-level back-to-back converters, it is not only necessary to control each converter, but also to suppress the zero-sequence circulating current between each converter. Therefore, it is of great significance to study the ZSCC suppression of parallel system of three-level back-to-back converters.

Scholars at home and abroad have done a lot of research on this. References [7] and [8] add hardware circuits to suppress the circulating current, but the volume and cost of the system are significantly increased. Hou [9] uses the harmonic elimination PWM method to achieve low-frequency ZSCC suppression. However, this method sacrifices part of the harmonic performance and has limited suppression effect on mid and high frequency circulating currents. The PI controller or deadbeat controller is used to distribute the zero vector action time in SVPWM modulation in [10] and [11], which can effectively suppress the circulating current. However, the parallel three-level converter hardly uses zero vector, and this control method is difficult to apply. In [12], a novel modular three-level inverter based on LCL filter is proposed to suppress the low-frequency zero-sequence circulating current by changing the operating time of the zero-sequence component. In [13], a small vector feed-forward control method with the PI controller is proposed to achieve circulating current suppression. However, the information of two inverters should be obtained in the control and it is not easy to expand.

This paper establishes an average model of zero-sequence circulating current for the paralleled back-to-back three-level converters. Based on the opposite effects of DPWM1 and DPWM3 on zero-sequence circulating current, this paper proposes a hybrid switching modulation strategy that uses DPWM1 and DPWM3 to realize the circulation suppression of parallel system based on the hysteresis controller. Finally, the accuracy and effectiveness of the proposed method are verified by experiments on a 10kW three-level back-to-back parallel experimental platform.

2. Averaged Model of Back-To-Back Parallel System of Three-level Converters

In the wind power generation system, the permanent magnet synchronous motor is connected to the grid through a three-level full-power converter connected in parallel, as shown in Figure 1. Two sets of converters share the DC bus.



Figure 1. Topology of paralleled three-level back-to-back converters.



Figure 2. Simplified topology of back-to-back converter.

To simplify the analysis, replace the permanent magnet synchronous motor with a symmetrical three-phase AC voltage source. As shown in Figure 2, a simplified single converter topology can be obtained. According to Kirchhoff's voltage law, the equivalent model of the parallel converters can be represented as:

$$\begin{cases} L_{mk} \frac{di_{mak}}{dt} + u_{amk} - u_{agk} + L_{gk} \frac{di_{gak}}{dt} = u_{mn} + e_{ma} - e_{ga} \\ L_{mk} \frac{di_{mbk}}{dt} + u_{bmk} - u_{bgk} + L_{gk} \frac{di_{gbk}}{dt} = u_{mn} + e_{mb} - e_{gb} \\ L_{mk} \frac{di_{mck}}{dt} + u_{cmk} - u_{cgk} + L_{gk} \frac{di_{gck}}{dt} = u_{mn} + e_{mc} - e_{gc} \end{cases}$$
(1)

where e_{mi} , e_{gi} (i=a, b, c) are grid voltage and motor voltage respectively; uimk, uigk(*i*=*a*, *b*, *c*) represent the output phase voltage of the machine side and the grid side of converter *k* respectively; u_{mn} is the voltage between the neutral point of the machine side and the grid side; L_{mk} and L_{gk} (*k*=1,2) are filter inductance; i_{mik} , i_{gik} (*k*=1, 2; *i*=*a*, *b*, *c*) respectively represent the three-phase current of the converter *k*.



Figure 3. Simplified topology of back-to-back converter.

Because the DC bus separates the machine side from the grid side, the circulating current on the machine side and the grid side are independent of each other. For the circulating current on the same side, the circulating currents of the paralleled converters are equal in magnitude and opposite in direction. Therefore, the ZSCC can be defined as:

$$\begin{cases} i_{mz} = i_{mz1} = \sum_{i=q,b,c} i_{mi1} = -\sum_{i=q,b,c} i_{mi2} = -i_{mz2} \\ i_{gz} = i_{gz1} = \sum_{i=q,b,c} i_{gi1} = -\sum_{i=q,b,c} i_{gi2} = -i_{gz2} \end{cases}$$
(2)

Summing the three-phase of (1):

$$\sum_{i=a,b,c} (u_{imk} - u_{igk}) + L_{mk} \frac{di_{mzk}}{dt} + L_{gk} \frac{di_{gzk}}{dt} = 3u_{mn}$$
(3)

The zero-sequence voltage can be expressed as:

$$\begin{cases} u_{zmk} = \sum_{i=a,b,c} u_{imk} \\ u_{zgk} = \sum_{i=a,b,c} u_{igk} \end{cases}$$
(4)

According to (2) and (4), When k = 1, 2, (1) can be simplified to:

$$\begin{cases} (L_{m1}+L_{m2})\frac{di_{mz}}{dt} = u_{zm2} - u_{zm1} \\ (L_{g1}+L_{g2})\frac{di_{gz}}{dt} = u_{zg2} - u_{zg1} \end{cases}$$
(5)

Then, the equivalent model of the back-to-back parallel converter can be obtained according to (5), as shown in Figure 3.

3. ZSCC Suppression Based on DPWM Hybrid Switching Modulation

The SVPWM of the three-level converter is composed of 1 zero vector, 6 small vectors, 6 medium vectors and 6 large vectors. Among them, there are redundant vectors in the small vectors and the zero vectors, as shown in Figure 4.

The selection of vectors in three-level SVPWM follows the NTV(Nearest Three Vector) principle, and both redundant small vectors are applied to reduce harmonics. When the reference vector locates on subsector I.1, the switching sequence of SVPWM is shown in Figure 5. T1, T2 and T3 represent the acting time of each vector respectively, and the redundant small vectors have the same action time.



Figure 4. Basic space vector of SVPWM.



Figure 5. Switching sequence of subsector I.1.

Due to the isolation of the DC bus, the ZSCC on the machine side and the grid side are independent of each other. Therefore, the ZSCC on both sides can be discussed separately, and the machine-side circulating current is taken as an example for analysis. According to(5), the circulating current is caused by unequal zero-sequence voltages between the two converters. In order to investigate the low frequency characteristics of the zero-sequence voltage, the average zero-sequence voltage(AZSV) should be calculated. The AZSV of subsector I.1can be expressed as:

$$AZSV_{I-1} = \frac{-\frac{T_1}{2} \frac{V_{dc}}{3} - T_3 \frac{V_{dc}}{6} + \frac{T_1}{2} \frac{V_{dc}}{6}}{T_s}$$
(6)

where the zero-sequence voltage amplitude of vectors onn, oon, ooo and poo are -Vdc/3,-Vdc/6,0 and Vdc/6 respectively.

Then, the AZSV of the reference vector passing through the entire vector space can be calculated. Figure6 is the waveform of AZSV within a fundamental period (f=50Hz). It can be seen that the AZSV of three-level SVPWM is the triple frequency component of the fundamental wave. According to(5), the harmonic frequency of circulating current should also be mainly composed of triple frequency.



Figure 6. AZSV of three-level SVPWM (modulation index m=0.8).



Figure 7. Modified switching sequence of machine-side converter 1.

For the paralleled two converters on the same side, the magnitude of the circulating current is the same, but the direction is opposite. Therefore, if the ZSCC of one converter is controlled, the circulating current of another converter is naturally controlled. The following analysis takes the ZSCC control of converter 1 as an example. The signs of the zero-sequence voltage amplitudes of the redundant small vectors in the three-level SVPWM are always opposite. Therefore, the effect of the redundant small vector on the AZSV in each switching cycle is also opposite according to(6). Without changing the output voltage of the SVPWM, the AZSV of the converter 1 can be adjusted by changing the action time of the redundant small vector, as shown in Figure 7. Where k is an adjustment factor for the action time of the redundant small vector. By changing the regulation factor k of the redundant small vector, the AZSV difference of the paralleled converters can be adjusted to zero to suppress the circulating current.

In continuous PWM modulation, the purpose of suppressing circulation can be achieved by adjusting the time of the redundant small vector of one of the converter SVPWM switch sequences to eliminate the difference between zero-order voltages of the two converters. However, in DPWM modulation, since there is no redundant small vector in the switch sequence, the method of zero-order circulation suppression by adjusting the action time of redundant small vector is no longer applicable. Therefore, it is also necessary to use the redundant switch sequence to the DPWM1 modulation strategy, the DPWM3 modulation strategy, to achieve the suppression of zero-order circulation.DPWM1 and DPWM3 are shown in Figures 8 and 9.



Figure 8. DPWM1.



Figure 9. DPWM3.

In each sector, the selection of redundant small vectors for both modulation strategies are always the opposite. According to the previous analysis, in the three-level converter space vector pulse width unified modulation model, when the allocation factor of redundant small vector k=1, that is, only the choice of P-type small vector, the average zero-order voltage in a switching cycle is the largest, and when k=-1, the average zero-order voltage of the three-level converter is the smallest. Therefore, the effect of DPWM1 and DPWM3 modulation strategies on zero-order circulation is always reversed at any time of vector modulation.

However, according to Figures 8 and 9, the value of redundant small vector allocation factor k in vector space of DPWM1 and DPWM3 is constantly switched between 1 and -1, that is to say, the effect of the circulation of DPWM1 and DPWM3 is not fixed and needs to be discussed in sectors. From the clamp interval distribution of DPWM1, it can be seen that in 1,3,5 small sectors of I, III, V sectors, the allocation factor k value of redundant small vectors is constantly taken 1, that is, only the P-type small vector is used, at this time the zero-order component is the largest, with a positive direction to increase the role of zero-order circulation, and in II, IV, VI large sector 2,4,6 small sectors, redundant small vector allocation factor constant set -1, that is, only used to N-type small vector, at this time the zero-order component is the smallest. It has the effect of increasing the zero-order circulation in a negative direction. The redundant small vector allocation ratio of the DPWM3 modulation strategy is completely complementary to DPWM1 in each sector, so the effect of DPWM1 and DPWM3 on zero-order circulation is the opposite at any moment.

Based on this, a zero-order circulation suppression method based on the hysteresis controller can be obtained, and the hybrid switching modulation strategy of DPWM1 and DPWM3 is still taken as an example, while the inverter 2 adopts the modulation strategy based on DPWM1. First of all, the sector where the reference vector is located is judged, when the reference vector is located in I, III, V large sectors of 1,3,5 small sectors, at this time the DPWM1 modulation strategy will increases the flow of the zero-order circulation to the positive direction, and DPWM3 modulation strategy will increases the flow of the zero-order circulation i_{zm} of the parallel converter, and switching the modulation strategy from DPWM1 to DPWM3 when the zero-order circulation i_{zm} reaches the upper threshold i_{zth} , thus reducing the zero-order circulation. When the zero-order circulation i_{zm} reaches the threshold lower limit $-i_{zth}$, switching the modulation strategy from DPWM1 to DPWM1 to DPWM1 to DPWM1 to DPWM1.

can increase the zero-order circulation (absolute value decreases), and the control principle of the circulation is shown in Figure 10.



Figure 10. The principle of hysteresis control of zero-order circulation.

In order to reduce the additional switching loss caused by switching modulation strategies, the switching time to select the end of each switching cycle, at the beginning of the switching cycle, the switching sequence of the DPWM1 and DPWM3 modulation strategies will only occur in one phase of the switching state transition. If the I-3 sector modulation strategy is switched from DPWM1 to DPWM3, the switch sequence conversion order is: poo->pon ->oon-> onn->->pon, only one-phase switching device in each switching losses. The analysis of the above-mentioned zero-order circulation suppression strategy is based on two parallel converters on the machine side, but for the two converters on the grid side, the above-mentioned circulation suppression method is also applicable.

4. Experimental Results

In order to verify the effectiveness of the ZSCC suppression strategy proposed in this paper, a back-to-back parallel system composed of four 10kW three-level converters was built for experimental verification. In the experiment, the motor is replaced by a three-phase AC source, which is still called "machine side" for clarity of expression. The machine-side converter adopts double closed-loop control to establish a stable DC voltage, while the grid-side converter uses current loop control to connect to the grid. The machine-side and grid-side voltage sources are separated by isolation transformers. The filter inductances on machine side and grid side are both 4mH; The upper and lower capacitors on the DC side are both 3300uF; Carrier frequency is 5kHz; DC voltage is 400V; The effective value of AC line voltage on machine side and grid side is 190V.

As shown in Figures 11 and 12, the experimental results are based on zero-order circulation suppression under the DPWM modulation strategy. Figures 11 (a) and 11 (b) are cases where the current of the two converters is given equal in parallel, and the reference current of the two converters is: $I_{ref1}=I_{ref2}=5A$, at which point the zero-order voltage of the two converters is basically inhibition, so that zero-order circulation is relatively small without circulation control shown in Figure 11 (a), and the distortion of the grid-connected current is not obvious, and Figure 11 (b) adds a stagnant-controlled circulation control method to show that the zero-order circulation is effectively

controlled. The output current of the converter has also been improved. Figures 12 (a) and 12 (b) give inconsistent currents to two converters, where the reference currents for the two converters are: $I_{ref1}=5A$, $I_{ref2}=10A$. Figure 12 (a) is a zero-order circulation control situation, at this time due to the current given inconsistency, the zero-order voltage of the two converters is very different, zero-order circulation is very obvious, the grid current also has a very large distortion; However, compared with systems with continuous PWM modulation strategies, parallel system current harmonic performance based on DPWM modulation strategies is slightly worse.



Figure 11. Experiment results with $I_{ref}=I_{ref}=5A$.(a) neither machine side nor the grid side with ZSCC control. (b)proposed DPWM Hybrid Switching Modulation Strategy.



Figure 12. Experiment results with Iref1=5A, Iref2=10A.(a) neither machine side nor the grid side with ZSCC control. (b)proposed DPWM Hybrid Switching Modulation Strategy.

5. Conclusion

In this paper, the zero-sequence circulating current model of three-level back-to-back parallel system is established, and the principle of ZSCC is analyzed based on the modulation method of SVPWM. Based on the opposite effects of DPWM1 and DPWM3 on zero-sequence circulating current, this paper proposes a hybrid switching modulation strategy that uses DPWM1 and DPWM3 to realize the circulation suppression of parallel system based on the hysteresis controller. Experimental results on 10kW converters platform verify the effectiveness of the proposed method. Results on 10kW converters platform verify the effectiveness of the proposed method.

References

- Nabae A, Takahashi I and Akagi H. A new neutral-point-clamped PWM inverter. IEEE Transactions on Industry Applications. 1981 Sept; IA-17(5):518-523.
- [2] Zhang X, Li M and Xu D. PCC voltage perturbation path analysis and compensation for grid-connected voltage-source converter under weak grid. IEEE Transactions on Industrial Electronics. 2021 Dec; 68(12):12331-12339.
- [3] Li W, Zhang X, Zhang F, et, al. Integrated modulation of dual-parallel three-level inverters with reduced common mode voltage and circulating current. IEEE Transactions on Power Electronics. 2021; PP(99):1-1.
- [4] Shao Z, Zhang X, Wang F, and Cao R. Modeling and elimination of zero-sequence circulating currents in parallel three-level T-Type grid-connected inverters. IEEE Trans. Power Electron. 2015 Feb; 30(2): 1050-1063.
- [5] Li W, Zhang X and Xu D. integrated modulation of dual-parallel NPC inverters with eliminated CMV. IEEE Transactions on Industrial Electronics. 2022 Aug; 69(8):8113-8122.
- [6] Zhang XG, Li W, Xiao Y, Wang G and Xu D. Analysis and suppression of circulating current caused by carrier phase difference in parallel voltage source inverters with SVPWM. IEEE Transactions on Power Electronics. 2018 Dec; 33(12):11007-11020.
- [7] Li W, Zhang X, Zhao Z, Zhang G, Wang G and Xu D. Implementation of five-level DPWM on parallel three-level inverters to reduce common-mode voltage and AC current ripples. IEEE Transactions on Industry Applications. 2020 July-Aug; 56(4):4017-4027.
- [8] Zhang C, Du S and Chen Q. A novel scheme suitable for high-voltage and large-capacity photovoltaic power stations. IEEE transactions on industrial electronics. 2013 Sept; 60(9):3775-3783,
- [9] Hou C. A multicarrier PWM for parallel three-phase active front-end converters. IEEE Transactions on Power Electronics. 2013 June; 28(6):2753-2759.
- [10] Zhang XG, Zhang WJ, Chen JM and Xu DG. Deadbeat control strategy of circulating currents in parallel connection system of three-phase PWM converter. IEEE Transactions on Energy Conversion. 2014 June; 29(2):406-417.
- [11] Zhang XG, Chen JM, Ma Y, Wang YJ and Xu DG. bandwidth expansion method for circulating current control in parallel three-phase PWM converter connection system. IEEE Transactions on Power Electronics. 2014 Dec; 29 (12):6847-6856.
- [12] Shao Z, Zhang X, Wang F and Cao R. Modeling and elimination of zero-sequence circulating currents in parallel three-level T-type grid-connected inverters. IEEE Transactions on Power Electronics. 2015 Feb; 30(2):1050-1063.
- [13] Xing X, Zhang Z, Zhang C, He J and Chen A. Space vector modulation for circulating current suppression using deadbeat control strategy in parallel three-level neutral-clamped inverters. IEEE Transactions on Industrial Electronics. 2017 Feb; 64(2):977-987.