Transdisciplinary Engineering: A Paradigm Shift
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A Concurrent Design Architecture for Electronic Product Design and Test

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Abstract. Concurrent Design (CD) has been applied in space missions and systems designs since the European Space Agency (ESA) evaluating the benefits of CD towards assessment studies as part of the definition for future space missions. In 1998, the European Space Research & Technology Centre (ESTEC) Concurrent Design Facility (CDF) was established to perform concurrent assessments of space missions. CDF approach is an alternative to the traditional design methods due to its abilities to address deficiencies such as, lack of synergy among design teams, inefficient design cycle, lack of systems-level perspective and developing a completely consistent design process. Research institutions, industries and universities using CDF/CE have reported better results than traditional methods for end-to-end space missions and space systems design projects. But, over the past 20 years, CDF/CEF has focused mainly in aerospace system design when compared with automotive and electronic products designs sectors. These commercial product design/manufacturing sectors are important to our global economy too, so CDF/CEF methods should also be widely expanded into these sectors. This should helps meet market windows, lower product costs with improved quality and reliability. In this respect, more engineers are required to be trained in CDF focusing in automotive and electronic products designs for production. This paper provides high level description of early CDF architecture, electronic volume production line architecture, and integrate the relevant parts of both to derive an enhance CD architecture. Next, the working principles of the main testing platform to capture production defects will be presented in order to show the benefits of incorporating design-for-testability (DFT) especially in the early CDF design phase, before providing an adaptation of this enhance CD version [1], suitable for education. This aims at familising students in the process of application of specific domain disciplines including design-for-manufacturability (DFM) and design-for-testability (DFT) for volume production.

Keywords. Concurrent Design Facility, Aerospace design education, Space missions and systems, Automotive engineering and Electronic Product Designs.

Introduction

Concurrent Design (CD) approaches have been applied in space missions and systems designs since the European Space Agency (ESA) evaluated the benefits of CD for future space missions [2]. The ESA Concurrent Design Facility (CDF) was established in 1998 to perform space missions assessments. The CDF approach is an alternative to the traditional design methods due to its abilities to address deficiencies such as, lack of synergy among design teams, inefficient design cycles, lack of systems-level perspective and developing a completely consistent design is difficult [3]. Research

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institutions, industries and universities using CDF have reported better results than the traditional methods for end-to-end space missions and space systems design projects.

This paper provides a high level description of the early CDF architecture and electronic production line architecture in Section 1 and 2 respectively. In Section 3, the working principle of a test platform to capture production defects is described in order to show the benefits of incorporating design-for-testability (DFT) especially in the early CDF design phase within the enhance CDF architecture (Figure 7). Section 4 provides an adaptation of the enhance CDF environment mainly for consumer electronic product and automative product design (target for volume production), which is also suitable for education. This is to familiarise students in the process of application of specific domain disciplines including design-for-manufacturability (DFM) and design-for-testability (DFT) for volume production.

1. Early CDF/CEF framework workflows

The CDF concept was first introduced by ESA for space mission design [2, 4, 5]. It started operation in early 2000, located in Noordwijk in the Netherlands. Its use to date has recorded a factor of 4 reduction in design time and a factor of 2 reduction in cost. increased no. of studies per year, quality improvement to provide quick, consistent and complete mission design, technical reports as part of specifications for industrial activities & capitalisation of corporate knowledge for further reusability [5, 6].

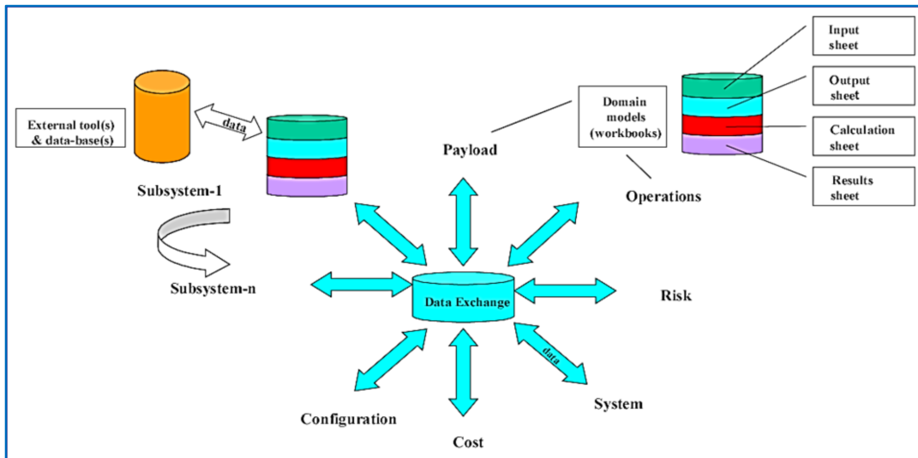

Figure 1. ESA/ESTEC CDF Architecture of Software Model [2].

The CDF process includes conducting model driven, highly co-operative and interactive design, which includes mission requirement analysis, mission analysis, subsystem design, designs verification, risk assessment and cost analysis, with design options comparison and trade-offs [5, 6]. The ESA CDF architecture is shown in Figure 1 [2].

2. Electronic Volume Production Line Architecture (PLA)

A typical electronic volume PLA is shown in Figure 2, which may consist of 8 main production stages. Production stage 2 and 3 may further consist of 3 sub-stages [1]. In general, a unit under production may consists of one or more Printed Circuit Board Assemblies (PCBA) housed in its associated chassis. Such PCBAs may typically use mixed technology, e.g. with topside Surface Mount Technlogy (SMT) and Plated Through Hole (PTH) components. After completing the main production stage 3 (Hand Load), the UUP will be transferred to the stage 4 (Test 1) to capture as much defects as possible. This is the In-Circuit-Test (ICT) platform, which determine the measured value against its set limit, one component at a time.

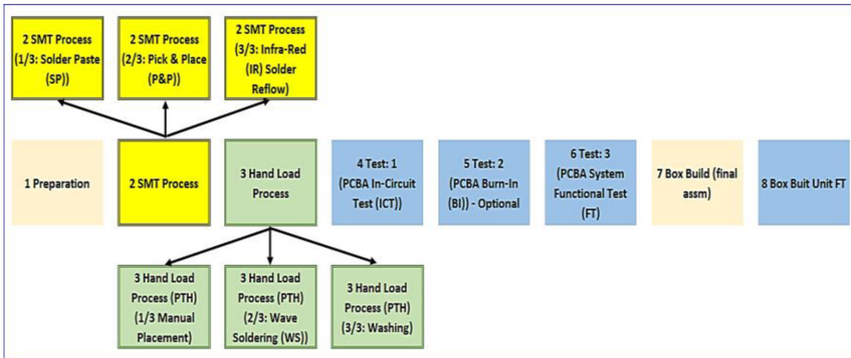

Figure 2. Volume Production Line Architecture (PLA) [1].

If the meaured value is outside the set limit, it is considered an ICT test reject. Subsequently, a team of engineers/technicians will debug the rejected PCBA to determine whether the reject was manufacturing/test equipment or process, or product design related. The ICT passed PCBAs are transferred to stage 5 for Burn-In (reliability test – optional). After that, the PCBA System Functional "black box" Test (SFT) commences at stage 6. After passing this stage, the PCBAs are assembled into their associated chassis manually.

3. Working Principles to Capture Production Defects

In volume production environments, it is critical that every completed PCBA is free of defect. In reality, this is a challenging task to accomplish due to 'land and estate' limitation versus the need to pack as many features as possible into the smallest PCBA size. Therefore, this is likely to impact the manufacturability and testability of the PCBA, and limits the ICT and SFT "black box" test platforms to capture production defects. Consequently, the producton lead time is longer, cost is higher with lower quality and reliability. This section describes the working principles of the ICT and SFT platforms for determining the values and limitations for capturing production defects from poorly designed PCBAs. These descriptions provide a generally good reference point for consideration when proposing an CDF architecture for education. The aim is to familiarise students with what needs to be considered when designing a product for volume production.

3.1. Working Principles of In-Circuit Test (ICT) Platform

This section describes the basic working principles of ICT test system measurements of SMT components bonded to a PCBA, its limitations and work-arounds relating to DFT. This highlights the importance to include a production test supporting domain discipline, amongst others production related disciplines, within the initial design phase. Only analog SMT component testing is described here. After the PCBA has been in-line washed, it is transferred into the ICT area for production stage 4 (ICT Test 1) to capture as many production process/equipment and/or design related defects as possible. Such defects may include open/short circuits, missing/wrong/reversed polarity/faulty components. The ICT test system measures each component at a time, while isolating surrounding components. For example, in Figure 3, the ICT measurement unit applies a known voltage and measures the current through R_{Ref} in feedback loop to determine the unknown resistance R_M. This is often called "apply voltage, measure current." [7]. R_M measured is accurate because there are no other components connected in parallel to R_M.

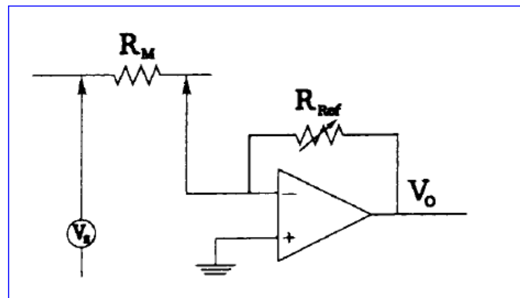

Figure 3. The "apply voltage, measure current" in-circuit measurement technique [7].

However, in many circuitries, parallel networks, such as those in Figure 4, are commonly used. So, the equivalent ICT measured value between X and Y using Eq. 1 is 6.67 kΩ though R1, R2 and R3 is 10 kΩ each. Under such conditions, the ICT test system is unable to measure the expected value of R1 accurately if the measurement point is only through a two-terminal X and Y nodes. In other words, it is unknown whether a 10 kΩ has actually been inserted/bonded or whether the 10 kΩ resistor is faulty.

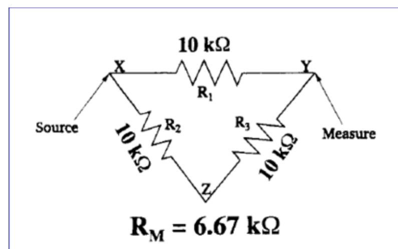

Figure 4. A measured value between X and Y of 6.67 kΩ is correct, while R1 is a 10 kΩ device [7].

$$\frac{1}{R_M} = \frac{1}{R_1} + \frac{1}{R_2 + R_3} \quad (1)$$

In such a scenario there are still two possible options available to determine that the 3 resistors are correct. Option 1 is to measure R1 accurately at 10 kΩ value. This is possible only if the ICT test system is able to assess node Z, i.e. via a hole used as test point on the bottle side of the PCBA – e.g. VIA hole is in Figure 6 (B)). If a Z node is available, the test engineer can include a guard point in the test programming instructions (Figure 5). The ICT test system is connected a ground node Z before measuring R1. In theory, there is no current flowing through resistor R2 or R3 because the Measurement point Y is at virtual ground and Z is at guard node ground, which is also at 0 V. Without voltage at the measure Y and guard node Z, there is no current flowing through both R2 and R3. This guarding at Z has effectively broken the parallel path and is said to have isolated the surrounding R2 and R3 from R1. All the source current from the known voltage source flows through R1 for an accurate measurement.

Option 2 measures R1, R2 and R3 together as a Block Circuit if the Z node is not assessible by the ICT test system on the bottom side of the PCBA. An example is shown in Figure 6 (C). The ICT measured value is 6.67 kΩ through point X and Y only. If this test fails, the debug technicians/engineers has to analyise all three components on the PCBA to determine the reject status. This takes longer than option 1, where only one component is analysed. It is important that the ICT test engineer collaborates with the PCB design engineer and circuit design engineer in the early design phase to optimise the block circuits test approach to assign test points.

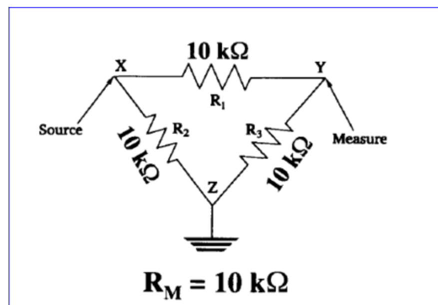

Figure 5. Grounds node Z before measuring R1. No current flows through resistors R2 or R3 [7].

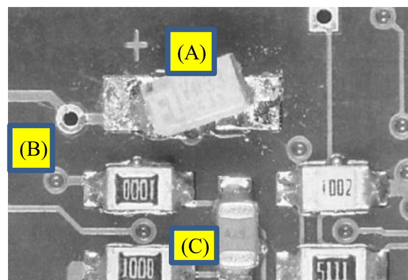

Figure 6. (A) An off-registration or off-pad component, (B) VIA holes linked to SMT pad/components allowing ICT test system to assess the SMT components for measurements and (C) notices that 2 SMT component pads is linked together without any visible VIA holes for use as test node [7].

The aforementioned ICT test principles and their limitations show the importance of facilitate testing in the design process. Poor ICT test coverage may result in the PCBA failing the System Functional Test (SFT). Such failure is generally more difficult to detect as SFT generally does identify a specific component failure. A PCB design engineer should always work closely with a circuit design engineer to optimise the test approach for circuitries that have little space on the PCB to assign VIA holes. Other considerations are VIA hole sizes and spacing. If a VIA hole size is too small, there may be contact problems due to mechanical accuracy. Large probes require a 1.0 mm hole and 2.5 mm spacing; it is able to reliably contact a 1.0 mm test pad for at least 10,000 connections. A smaller probe needs a 0.5 mm hole and 1.3 mm spacing. It is not as strong and is considered reliable for only 2,500 connections to a 0.5 mm pad [8].

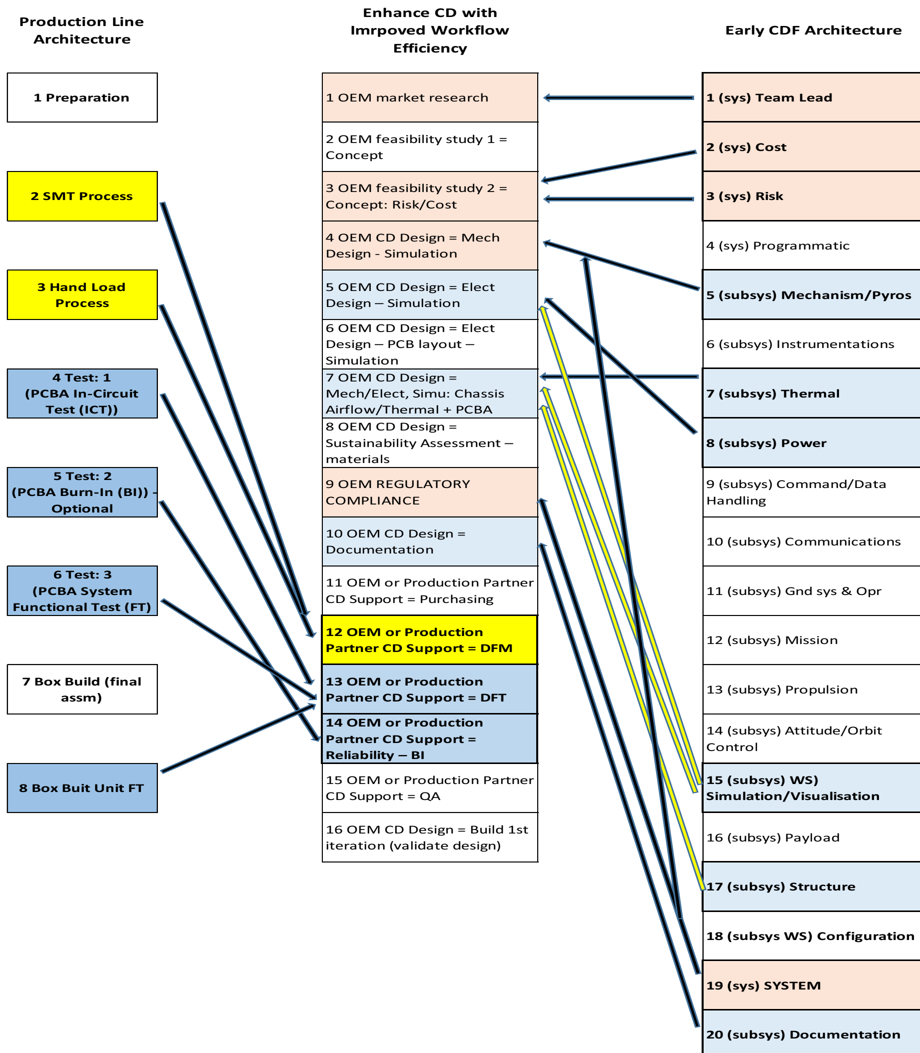

Figure 7. A CDF Architecture derived from a Production Line Architecture using relevant domain disciplines.

A CDF environment for electronic product design/manufacturing, e.g. consumer computer and automative audio/video/navigation with 16 domain disciplinesfor full product design cycle is shown in Figure 7. This new CDF environment includes production support in early design phase (middle column workflow) , derived from the relevant parts of Production Line Architecture (left column workflow) and early CDF Architecture (right column workflow). The advantages of this approach, which creates a new CDF environment with improved workflow efficiency is that, the first iteration design is unlikely to require further iterations re-design because potential manufacturing/test related defects were identified and resolved early in the 1st iteration design phase by production support specialists at almost real-time basis to the PCB design and other related design specialists. This is likely to provide better consistency in overall designed product performance, leadtime and lower production costs [1].

However, this approach is only workable if the selected supporting specialists are fully familiar with the complete specific capital production/test equipment operational limits and process limits which the targeted product is to be produced within it. The idea is to 'wrap' the product design around a specific production line environment, where each supporting specialist determines what the design configuration/limits are or are not workable within the targeted/selected specific production line process and equipment. Therefore, information required to determine manufacturability and testability comes from the extensive hands-on experience of each supporting domain specialist aligned to specific production processes. Such experience is also non-product specific, but mainly capital production/test equipment and process specific [1].

4. Adaptation of the enhance CDF Environment for Education

For educational purpose, smaller student team is more manageable and better suited [5]. The 16 domain disciplines can be reduced to 10 domain disciplines as in Figure 8. This effectively remove disciplines from Figure 7 considered less essential for familiarising students with CDF setting and process of application of specific domain discipline such as market research, sustainability assessment, materials, regulatory compliance, purchasing, QA and Build 1st (validate design) prototype. Common design software is to be used so that all stations could peer review almost realtime and provide quick feedback. Collaboration is by Email, MS Office, Skype video conference, realtime messaging and Cloud. Data/design models backup is by data exchange server and consolidation of sub-system and system level results is by spreadsheets and in-session discussions is by a large media wall and smart board.

2 OEM feasibility study 1 = Concept	3 OEM feasibility study 2 = Concept: Risk/Cost	4 OEM CD Design = Mech Design - Simulation	5 OEM CD Design = Elect Design – Simulation	6 OEM CD Design = Elect Design – PCB layout – Simulation	7 OEM CD Design = Mech/Elect, Simu: Chassis Airflow/Thermal + PCBA	10 OEM CD Design = Documentation	12 OEM or Production Partner CD Support = DFM	13 OEM or Production Partner CD Support = DFT	14 OEM or Production Partner CD Support = Reliability – BI

Figure 8. 10 Domain Disciplines in a CDF Architecture for Education.

Our approach, which adopt our proposed CDF integrated design environment (IDE), similar CDF layout and considerations of other CDF best practises/challenges described in detail in [5], do also have similarities to the approach adopted by [9], which is lesser, i.e. 10 essential study/domain discilines, is considered sufficient for educational purposes as the focus is mainly on familiarising students with the process

of applications of specific domain descriplines and not on actual continuous product developments. In this light, limitations described in section 3 is therefore not as critical for education (i.e. this approach only works if selected support specialists are fully familiar with the complete specific capital production/test equipment operational limits and process limits which the targeted product is to be produced.) Students are likely to acquire richer experiences in in-session design, almost-realtime collaborations internally [10], externally with other institutions, working together with every team members on the same pages, improving efficiency and completing the design projects with higher quality, shorter leadtime and less likely for re-design mainly due to DFM/DFT problems as presented in section 3.

5. Conclusions

In section 3, we have demonstrated that integrated production support domain disciplines is an important part in a CDF environment and should be an integral part of the initial design cycle in order to minimise the chances of re-designing due to mainly DFM/DFT problems. In section 3, we have also presented an enhanced CDF architecture derived from PLA and early CDF architecture, and proposed a CDF architecture in section 4, by adapting the enhance CDF architecture, with a reduced number of domain disciplines to accommodate smaller student teams. This is considered sufficient for education purposes as the aim is to familiarise students with the process of applying specific domain disciplines in a CDF environment with focus in consumer electronic product and automotive product design. This adaptation of a CDF environment is beneficial to students and the general electronic product and automotive industries as more such students are trained, and has the potential to become an invaluable tool for education.

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